Introduction

The demands over recent years by customers for increased quality and service will continue for the future. For this reason, several years ago Telefunken Semiconductors implemented a review of its quality systems with a view to improve its quality and reliability until it achieved “zero defect level” quality.

This means that it is no longer possible to ‘test-in’ the quality but instead it has to be ‘built-in’ at the design stage. An extensive effort was therefore required – covering research, development, production and administration. New tools were introduced to help in this process.

- Quality Function Deployment (QFD)
  – to determine customer requirements
- Failure Mode and Effects Analysis (FMEA)
  – to determine potential failure hazards
- R&R- (Repeatability and Reproducibility) tests – to look at the adequacy of our measurement techniques
- Up-Time Control (UTC) – for machines
- Statistical Process Control (SPC)
  – for control of processes
- Design of Experiments (DOE)
  – to help engineers be more productive in their work

Telefunken Semiconductors believes that quality of service is equally as important as the technical ability of its products to meet specified limits of performance and reliability.

- Short reaction time to customer’s questions
- Application support
- Fast complaint handling
- Customer partnership and service

are equally part of the quality objectives.

The quality improvement process is central to an integrated quality program designed to meet high quality objectives. This Total Quality (TQM) program involves all members of the company starting and driven by the companies’ top management.

The implementation of TQM has fundamentally changed the structure and tasks of Quality Assurance within the company. Previously production and quality had separate responsibilities, with production responsible for producing and quality responsible for the quality of the products. Today everybody is responsible for quality. It is the basic characteristic of every single process from design to delivery and beyond. The responsibility is not localized to a few steps but is an integral part of the complete process sequence.

Quality Management (QM) now mainly revolves around the development and implementation of new procedures and methods of TQM, the continuous setting of new quality objectives, the organisation and performance of audits and service to the customer in terms of quality issues.

This brochure acts as an introduction to this TQM process which is the essential means to achieve the goal of “zero defects”. The current results are also given. Explanations and calculated examples explain how these have been arrived at and show how to use quality statistics such as AOQ, EFR and LFR.

It is hoped that this information will demonstrate Telefunken Semiconductors’ quality policy and contribute to many customer/ supplier partnerships.

Quality Management System

Quality Policy TEMIC

Our goal is to achieve total customer satisfaction through everything we do. Therefore, the quality of our products and services is our number one priority.

Quality comes first!

All of us at TEMIC are part of the process of continuous improvement.

Figure 1. ‘Quality Policy TEMIC’

Telefunken Semiconductors’ four commandments (according to Phil B. Crosby) are:

1. **Quality means conformance not elegance.**
2. **It’s always cheaper to do the job right first time.**
3. **The only performance standard is “zero defects”.**
4. **The only performance indicator is the cost of quality.**

Total Quality Management (TQM)

TQM is a management system, centered on quality, based on the participation of all employees. It is aimed at long term success through customer satisfaction. It benefits the members of the organization and society in general [(DIN) ISO 8402].

Four Elements are Fundamental for Total Quality Management:

- Management commitment and example
- Quality Management System (QMS)
- Quality tools
- TQM-components

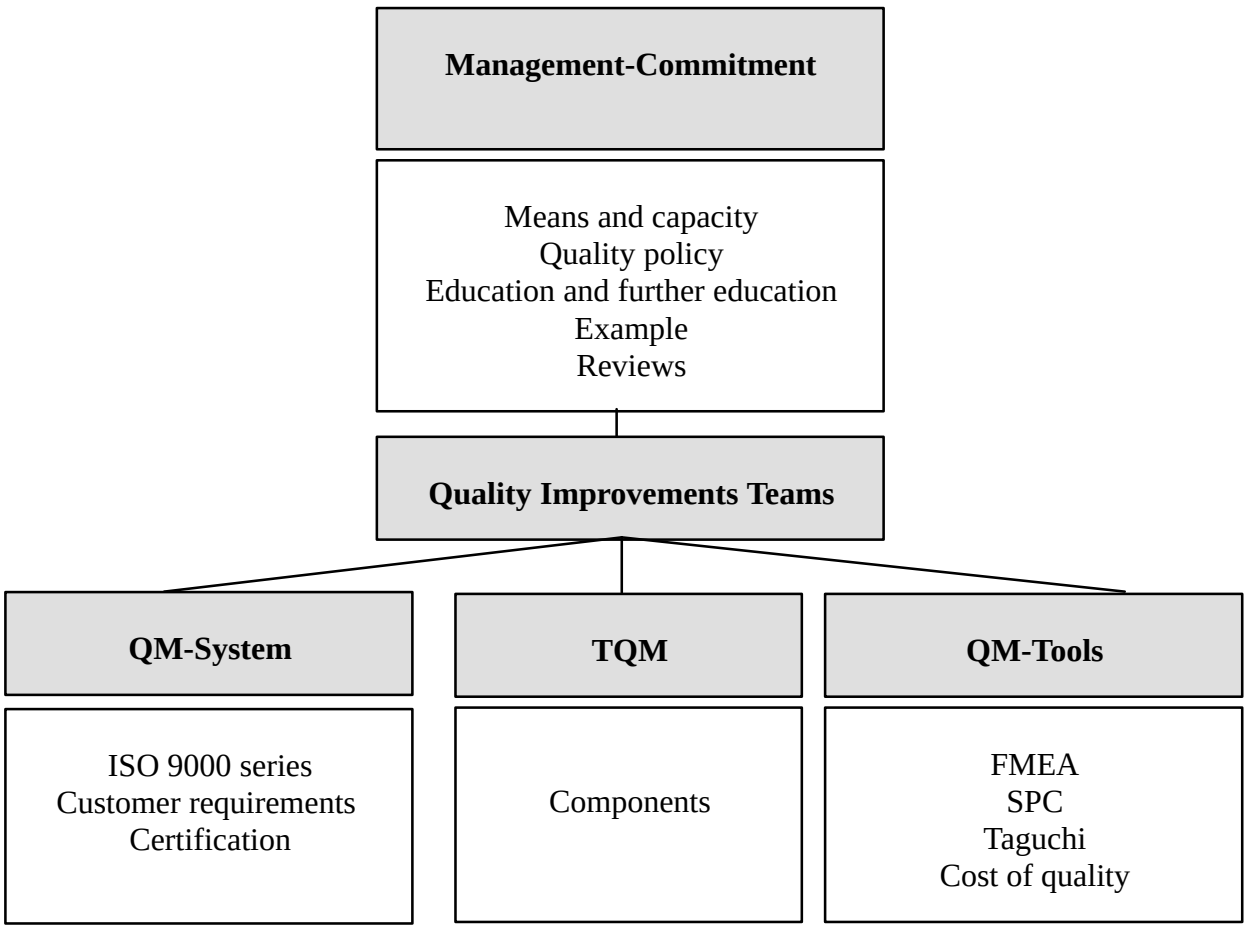


Figure 2. TQM-building [Masing, 'Handbuch Qualitätsmanagement']

Continuous Quality Improvement Process (QVP)

QVP Training

Telefunken Semiconductors' employees are trained in the understanding of TQM (according to their job in terms of content and depth of knowledge). The implementation of the quality improvement process is the responsibility of the Quality Management Department.

This is based upon:

- Quality is meeting the agreed requirements
- Failure analysis – preventive action
- "Zero defect" mentality
- Cost of quality
- Customer-supplier-relationships

Customer-Oriented Arrangement of All Employees

One essential goal of Telefunken Semiconductors is a pro-active approach to customer relations. This requires improving co-operation with customers in all aspects of the relationship. The starting point is to consider the quality of the products and services from the customer's point of view.

Quality Function Deployment (QFD), which is a systematic method for the collection and evaluation of customers needs and requirements, is the basis for evaluation.

In the framework of QVP there is no difference between internal and external customers. Everybody is a supplier as well as a customer and should define his requirements, as well as feedback information on whether the requirements are met or if there is any deviation.

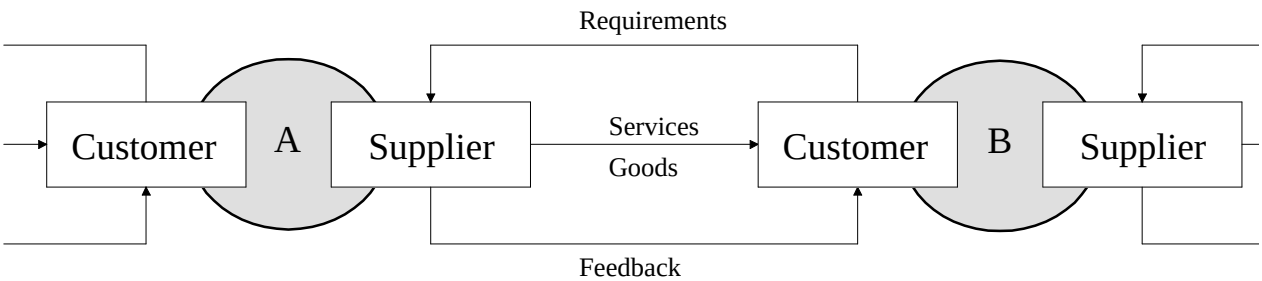


Figure 3. Everybody is a supplier and a customer

This unified progression defines every kind of job as a process (i.e., as a sequence of steps) which have a result.

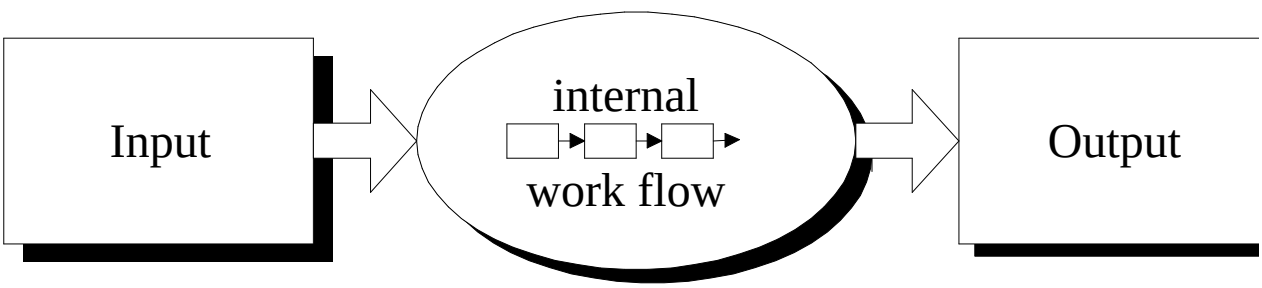


Figure 4. Each work is a process

A process may be divided into several sub-processes which have suppliers and customers. Each process has an output which should meet the requirements the customer expects. The customer's requirements therefore are needed as input.

Job-related education and training needs are determined by survey and included in a training program. Internal and external trainers or organizations perform this education and training.

Cost of Quality

In the framework of TQM and QVP, within Telefunken Semiconductors, the costs of quality are determined. 'Cost of quality' is defined as the difference between the price of non-conformance and the price of conformance. The price of non-conformance is defined as the avoidable costs (e.g., costs of complaints). The price of conformance includes preventive action (e.g., test and approval costs). The costs of quality are determined and analyzed by individual departments.

Top Management is regularly informed and sets the goals. One essential goal is the "zero defect" requirement for the quality of the delivered product.

Audit and Certification

The organisational methods, by which Telefunken Semiconductors assure quality, are laid down in the Quality Management Manual and cover the demands of known requirements such as ISO 9001, EN 29001. They guarantee that the organizational, commercial and technical activities which affect quality are performed in a planned, controlled and monitored manner.

ISO 9000 defines fundamental terms. It serves as a guideline for selection and implementation of procedures and defines the method of quality management.

ISO 9001 describes the model for quality assurance in design/ development/ production/ installation and servicing.

ISO 9002 corresponds to ISO 9001 without the range of quality assurance in design/ development.

All locations of Telefunken Semiconductors have been certified according to ISO 9001 or ISO 9002:

- The Heilbronn facility was certified in July 1993. This was confirmed by the certification institute with a re-audit in August 1994.
- The Vöcklabruck (Austria) facility was certified in May 1993. This was confirmed by the certification institute with a re-audit in June 1994.
- The Manila (Philippines) facility was certified in the first quarter 1994 according to ISO 9002.

VDE PRÜF- UND ZERTIFIZIERUNGSINSTITUT
Verband Deutscher Elektrotechniker (VDE) e.V.

CERTIFICATE

Registration-Number: 4226.10/QM/07.93 (AA)

This is to certify that the company

TEMIC Telefunken microelectronic GmbH
in the following location
Theresienstraße 2, D-74072 Heilbronn

has implemented and maintains a
Quality-Management System for the following scope:

Semiconductor

This QM-System complies with the requirements of:

ISO 9001; 1987, BS 5750 Part 1; 1987
Quality systems
Model for quality assurance in design/development, production, installation and servicing

This certificate is valid until July 31, 1996.

VDE Testing and Certification Institute
Department Certification

i.V. Hoeveler

D-63069 Offenbach/Main, Merianstraße 28
Date: 12.07.1993

The VDE Testing and Certification institut is accredited by DAR according to EN 45012.

Deutscher Akkreditierungsrat DAR TGA-ZO-009/92-00

Figure 5. ISO 9001 Certificate Heilbronn

VDE PRÜF- UND ZERTIFIZIERUNGSINSTITUT

CERTIFICATE

TEMIC Telefunken microelectronic GmbH
in the following location
Telefunkenstraße 5, A-4840 Vöcklabruck

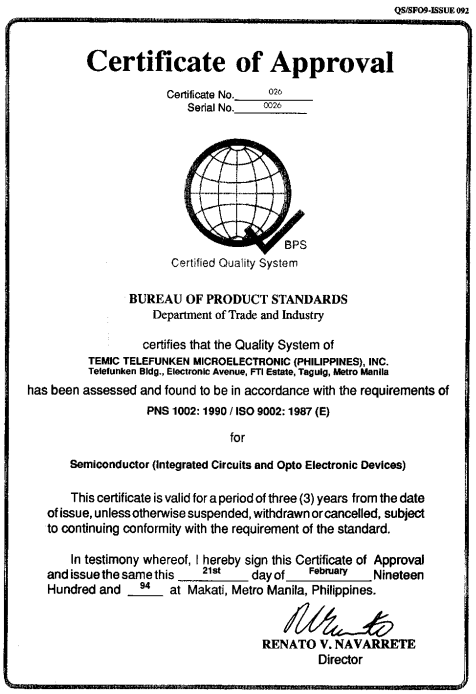
Discrete Semiconductor Devices

DIN ISO 9001; 1978, BS 5750 Part 1; 1987
Quality systems
Model for quality assurance in design/development, production, installation and servicing

VDE Testing and Certification Institute
Department Certification

DAR

Figure 6. ISO 9001 Certificate Vöcklabruck



QS/SFO9-ISSUE 092

Certificate of Approval

Certificate No. 026
Serial No. 0026

BPS
Certified Quality System

BUREAU OF PRODUCT STANDARDS
Department of Trade and Industry

certifies that the Quality System of
TEMIC TELEFUNKEN MICROELECTRONIC (PHILIPPINES), INC.
Telefunken Bldg., Electronic Avenue, FTI Estate, Taguig, Metro Manila
has been assessed and found to be in accordance with the requirements of
PNS 1002: 1990 / ISO 9002: 1987 (E)
for
Semiconductor (Integrated Circuits and Opto Electronic Devices)

This certificate is valid for a period of three (3) years from the date of issue, unless otherwise suspended, withdrawn or cancelled, subject to continuing conformity with the requirement of the standard.

In testimony whereof, I hereby sign this Certificate of Approval and issue the same this 21st day of February Nineteen Hundred and 94 at Makati, Metro Manila, Philippines.

RENATO V. NAVARRETE
Director

Figure 7. ISO 9001 Certificate Manila

Internal and external audits

The quality management system is periodically audited by an accreditation organization and by important customers. Internal audits are additionally performed with a view to continuous monitoring and improvement.

These internal audits are initiated by the head of the Quality Management Department on behalf of the board of management. The inspection takes place in accordance with a documented plan. This plan is issued at the beginning of each year and is continuously updated. The audit is carried out by a team and is based upon questionnaires which, if necessary, may be extended by the auditors. The result of the audit is summarized and forms – together with the corrective measures – an audit report which is distributed to responsible persons in the audited department, the head of QM and the Telefunken Semiconductors' board of management.

The auditors are employees trained by external organizations. At least one member of the team is independent from the department being audited.

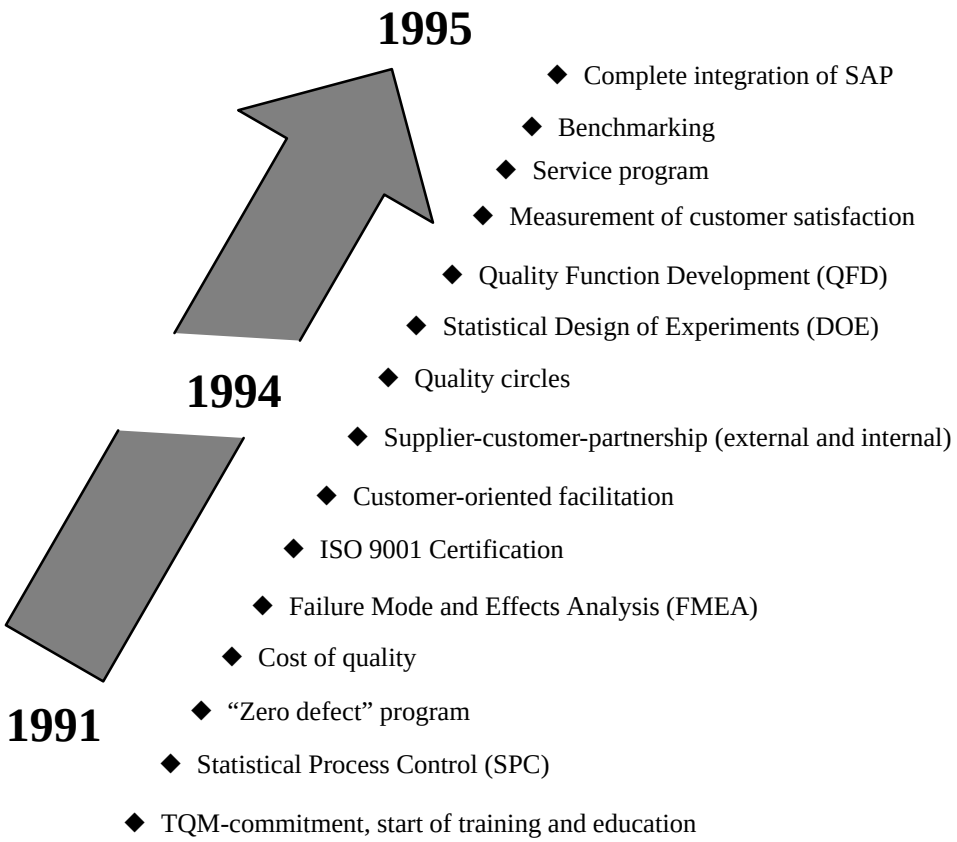


Figure 8. Telefunken Semiconductors' reached and future objectives

Quality Management Department

The Quality Management Department was reorganized in 1993. It is separated into Quality Systems, Customer Service and Products. The Vöcklabruck and Manila facilities have their own quality departments. QM-Vöcklabruck is responsible for diodes and transistors, QM-Manila is responsible for opto components. These departments report to QM-Heilbronn. All general procedures for qualification and reliability testing are centrally issued by QM-Heilbronn.

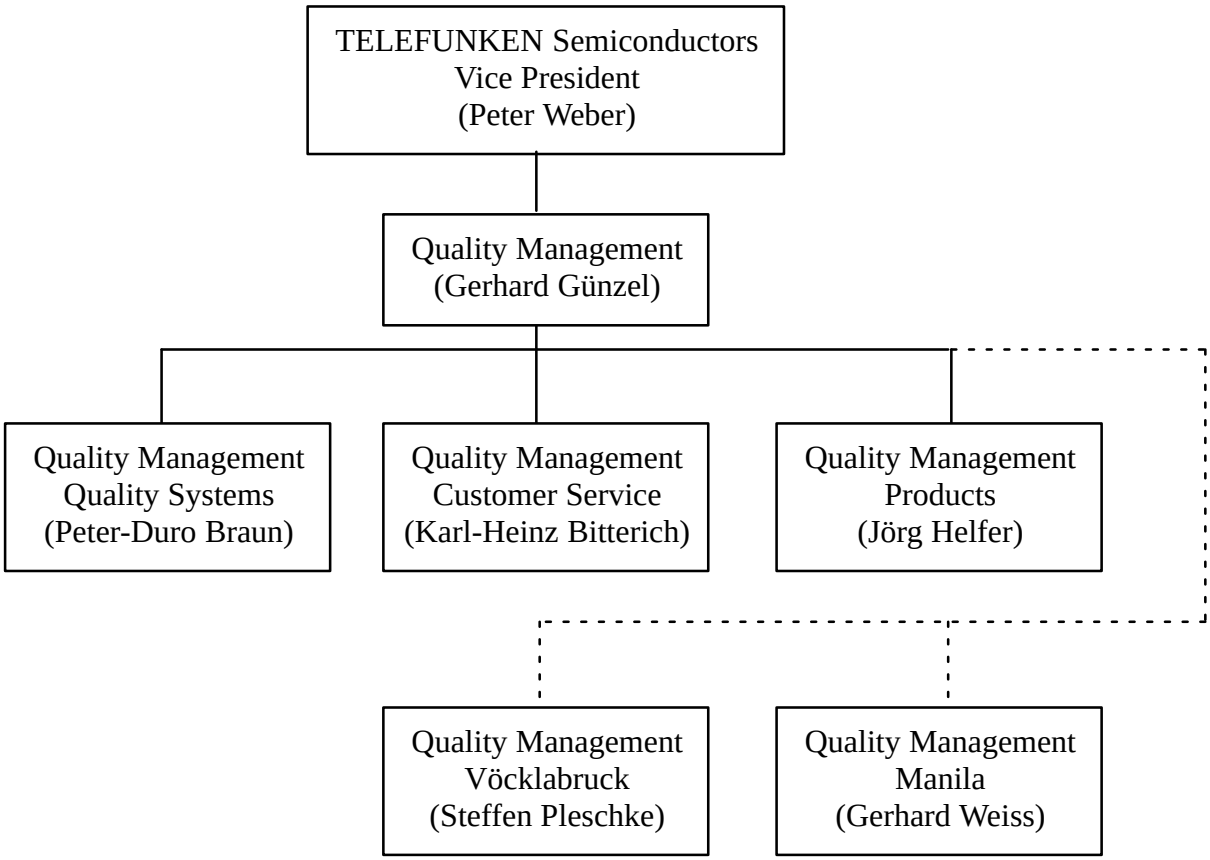


Figure 9. Structure of QM-department

Responsibilities

Quality Management

Subordinate to the Telefunken Semiconductors management. Responsible for

- Planning and monitoring QM-measures
- Qualification and release of products
- Product observation
- Evaluating information from product observations and, if necessary, implementing corrective measures
- Coordination of QM-measures with subsidiaries in Vöcklabruck and Manila
- Member of the TEMIC Quality Committee for definition and implementation of TQM TEMIC – worldwide

Quality Management Quality Systems

- Maintenance of the internal quality management system, coordination and implementation of internal and external audits
- Coordination of calibration
- Information and initial training for new quality tools
- Training in TQM

Quality Management Customer Service

- Customer service worldwide
- Customer visits in house, visits to customers' sites
- Strengthening quality partnerships with customers
- Insurance problems and product liability
- Coordination with other TEMIC Semiconductor divisions

Quality Management Products

- Qualification of new products, packages and wafer processes
- Release of product and process changes
- Coordination with other TEMIC Semiconductors divisions
- Electronic Data Processing (EDP) for Quality Management

Qualification and Release

New wafer processes, packages and device types are qualified according to the internal Telefunken Semiconductors specification QSA 3000.

QSA 3000 consists of five parts:

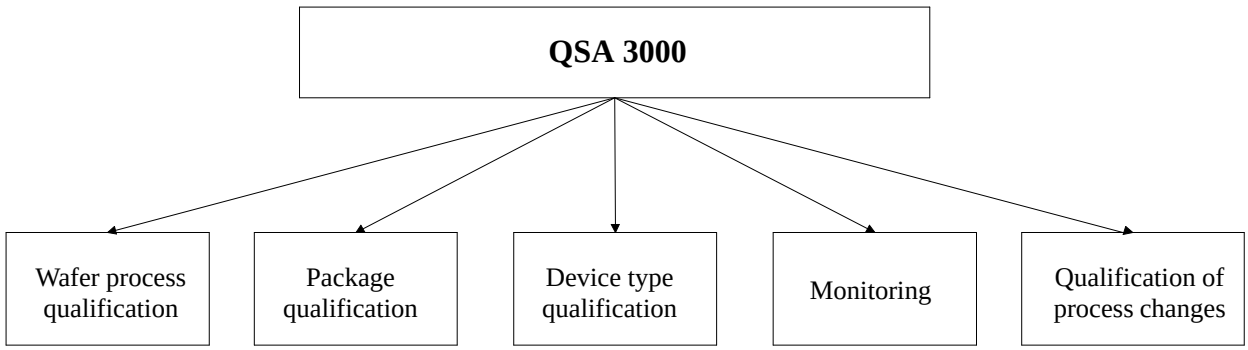


Figure 10. Structure of QSA 3000

Wafer process release: The wafer process release is the fundamental release/qualification for the different technologies used by Telefunken Semiconductors. Leading device types are defined for different technologies. Three wafer lots of these types are subjected to an extensive qualification procedure and are used to represent this technology. A positive result will release the technology.

Package release: The package release is the fundamental release/qualification for the different packages used. Package groups are defined. Critical packages are then selected; three assembly lots are subjected to the qualification procedure representing that package group. A positive result will release all similar packages.

Device type release: Device type release is the release of individual designs.

Monitoring: Monitoring serves both as a continuous monitoring of the production and as a source of data for calculation of early failures (early failure rate).

Release of engineering changes: All product or process changes are released by qualification according to stipulations (see following page).

Test procedures utilized are IEC 68-2-... and MIL-STD-883 D respectively.

Reliability tests are performed according to the following procedure:

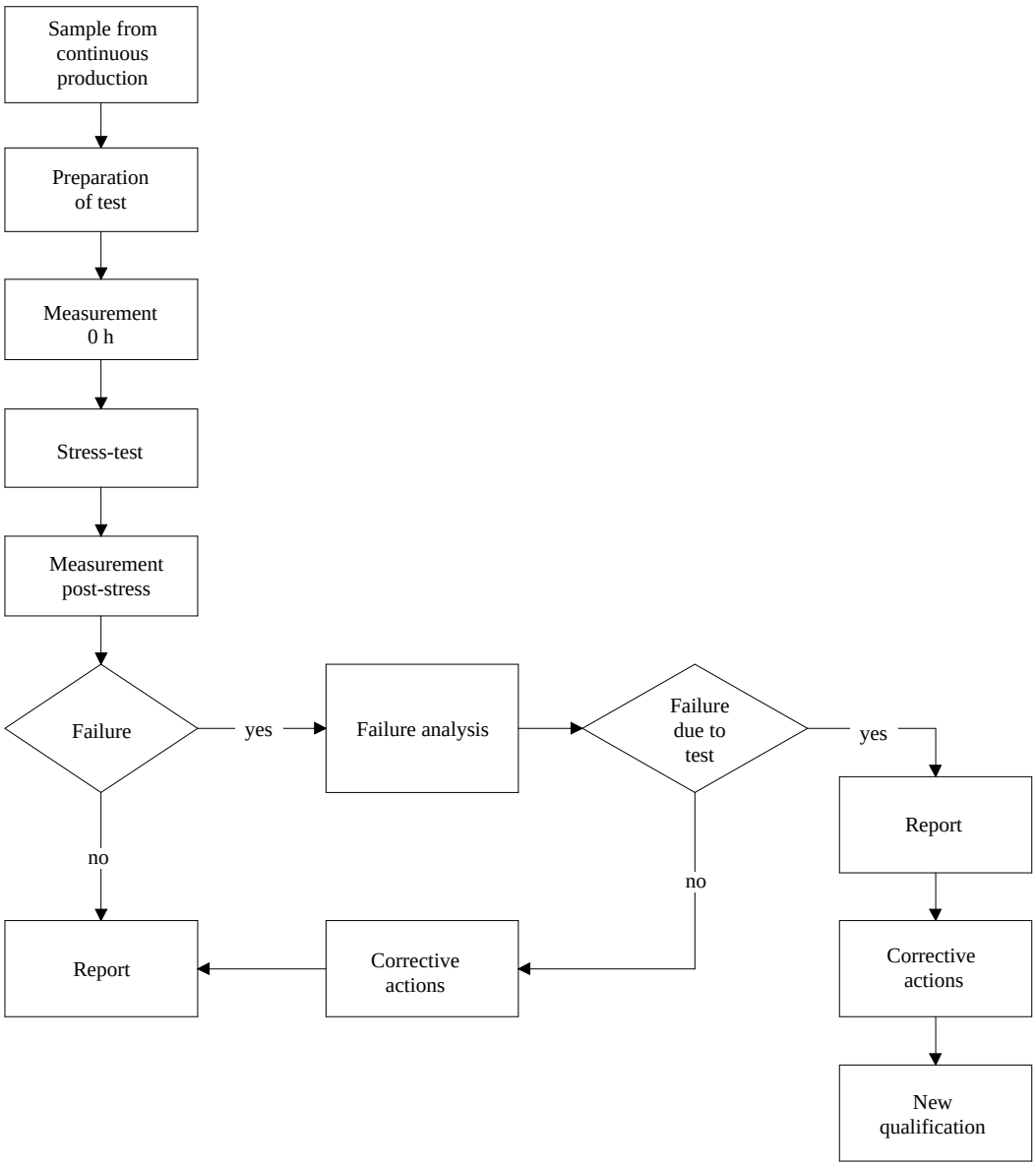


Figure 11. Procedure qualification tests

Product or process changes are released via ECN (Engineering Change Note). This includes proving process capability and meeting the quality requirements. Release requires approval from Design/Development, Production, Quality Management and Marketing.

In the case of essential changes (‘major changes’), customers are informed via Marketing before implementation. If stipulated in specific agreements, customer approval may also be required before implementation.

All parts are 100% tested after wafer production and assembly (both of which are SPC controlled) at final test. This is followed by a sample inspection. If failures occur during sample inspection, the lot is re-worked (depending upon the failure mode) and will then be returned for re-inspection. Only lots without failures are released to stock for delivery.

Production Flow

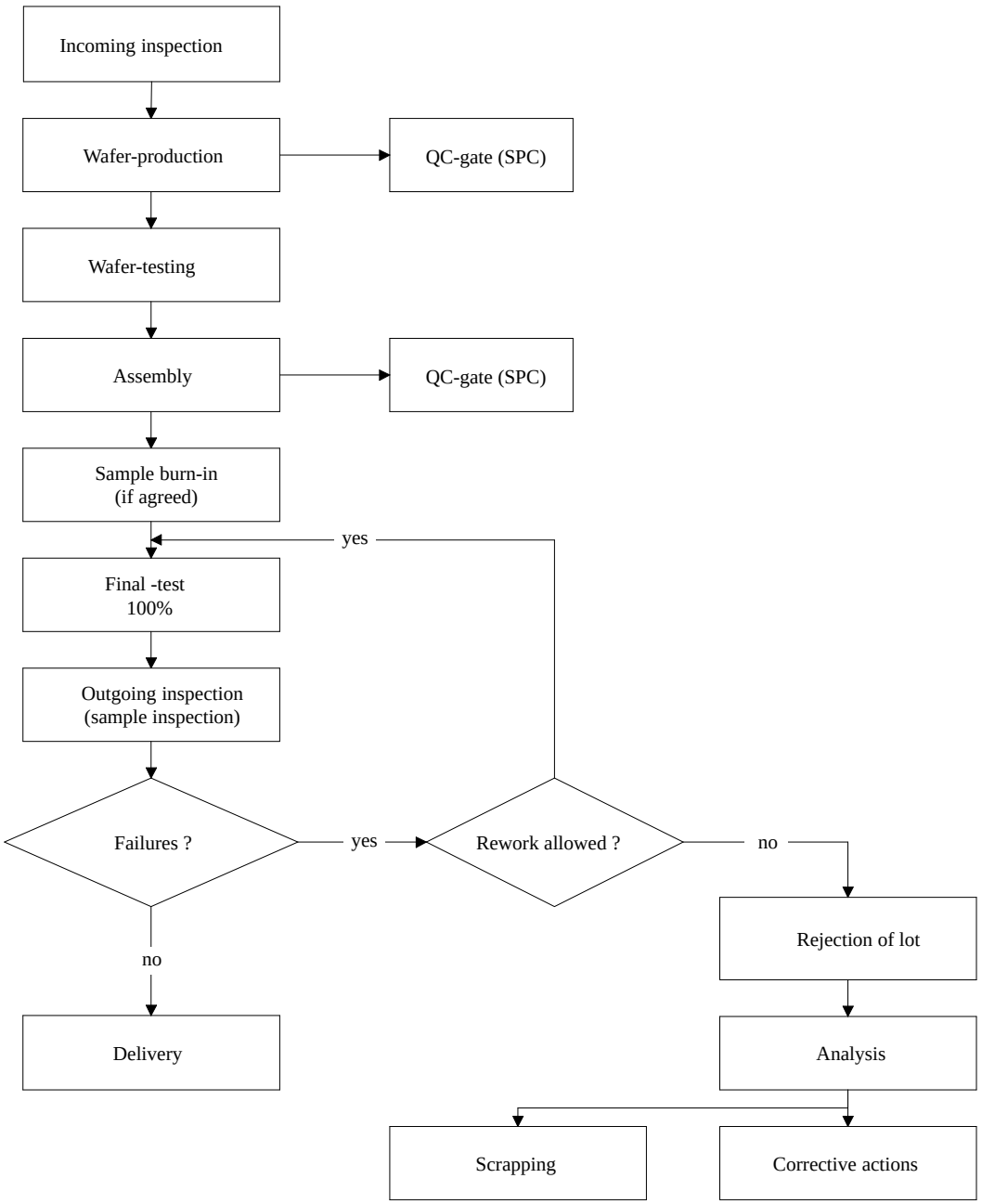


Figure 12. Production procedure

Complaints Handling

Customers' complaints are forwarded to the appropriate Sales department.
Exact and complete information from the customer concerning the failure is a valuable aid and accelerates the performance of the failure analysis.
After receipt of the parts, failure analysis is immediately performed, starting with electrical verification.

The customer receives at best

within 4 days (working days)	receipt confirmation and result of electrical verification (if measuring is possible at receiving location)
within 10 days	intermediate report of analysis
within 20 days	analysis report including corrective action

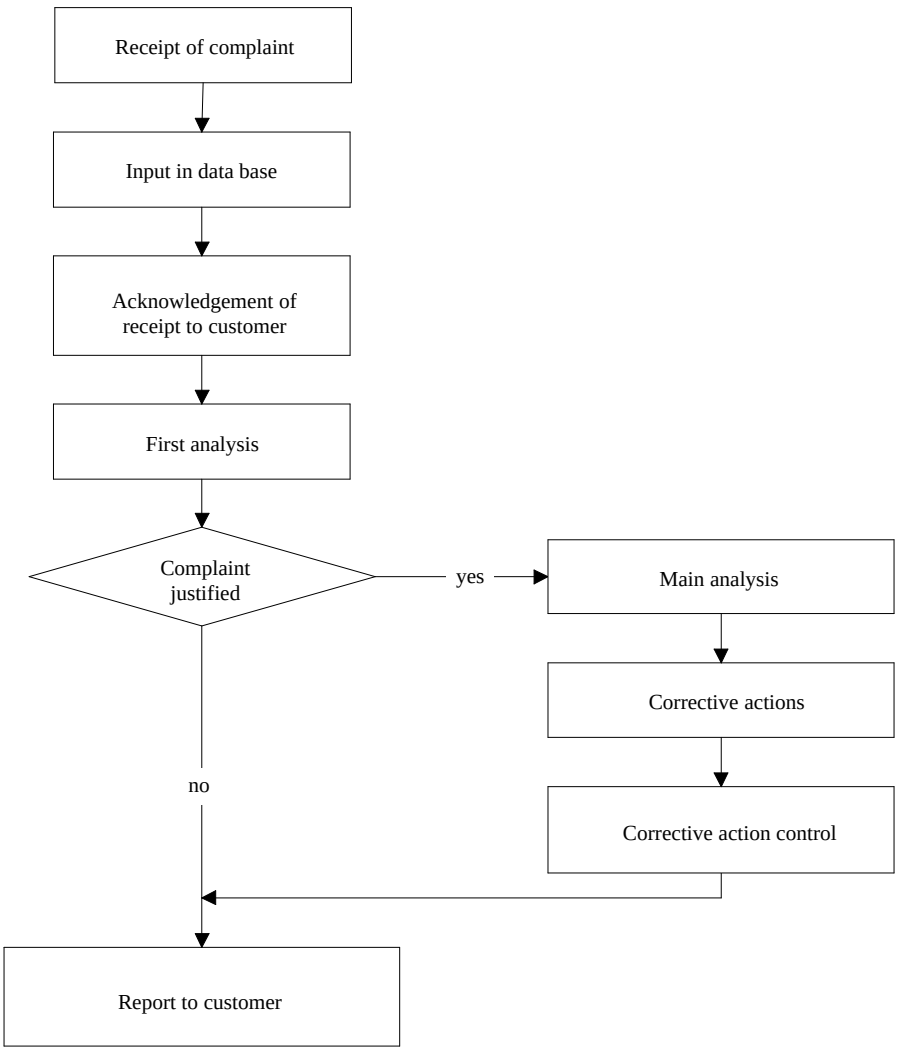


Figure 13. Procedure for handling complaints

An extensive and documented failure analysis is carried out for justified complaints.

Statistical Methods for Prevention

To manufacture high-quality products, it is not sufficient controlling the product at the end of the production process.

The quality has to be ‘designed-in’ during process- and product development. In addition to that, the ‘designing-in’ must also be ensured during production flow. Both will be achieved by means of appropriate measurements and tools.

- Statistical Process Control (SPC)
- R&R- (Repeatability and Reproducibility) tests
- Up-Time Control (UTC)
- Failure Mode and Effect Analysis (FMEA)
- Design Of Experiments (DOE)
- Quality Function Deployment (QFD)

Telefunken Semiconductors has been using SPC as a tool in production since 1990/91.

Using SPC, deviations from the process control goals are quickly established. This allows control of the processes before the process parameters run out of specified limits. To assure control of the processes, each process step is observed and supervised by trained personnel. Results are documented.

Process capabilities are measured and expressed by the process capability index (C_{pk}).

Validation of the process capability is required for new processes before they are released for production.

Before using new equipment and new gauges in production, machine capability (C_{mk} = machine capability index) or R&R (Repeatability & Reproducibility) is used to validate the equipment’s fitness for use.

Up-time is recorded by an Up-Time Control (UTC) system. This data determines the intervals for preventive maintenance, which is the basis for the maintenance plan.

A process-FMEA is performed for all processes (FMEA = Failure Mode and Effect Analysis). In addition, a design- or product-FMEA is used for critical products or to meet agreed customer requirements.

Design of Experiments (DOE) is a tool for the statistical design of experiments and is used for optimization of processes. Systems (processes, products and procedures) are analyzed and optimized by using designed experiments.

A significant advantage compared to conventional methods is the efficient performance of experiments with minimum effort by determining the most important inputs for optimizing the system.

As part of the continuous improvement process, all Telefunken Semiconductors’ employees are trained in using new statistical methods and procedures.

Identification and Traceability

Identification and traceability of Telefunken Semiconductors’ products is accomplished by using product marking. In the case of unmarked devices, this is marked on the packaging.

The marking as a minimum includes the part number, and if the area is sufficient, additional information such as assembly location and date. This data is also marked on the packaging. From this data, conclusions may be drawn as to the used materials, processes, procedures and inspections for the lots during wafer production and assembly.

Traceability in production is assured with lot travellers and working step sequence plans (AGAFs).

Reliability

The requirements concerning quality and reliability of products are always increasing. It is not sufficient to only deliver fault-free parts. In addition it must be ensured that the delivered goods serve their purpose safely and failure free, i.e., reliably. From the delivery of the device and up to it's use in a finished product, there are some occasions where the device or the finished product may fail despite testing and outgoing inspection.

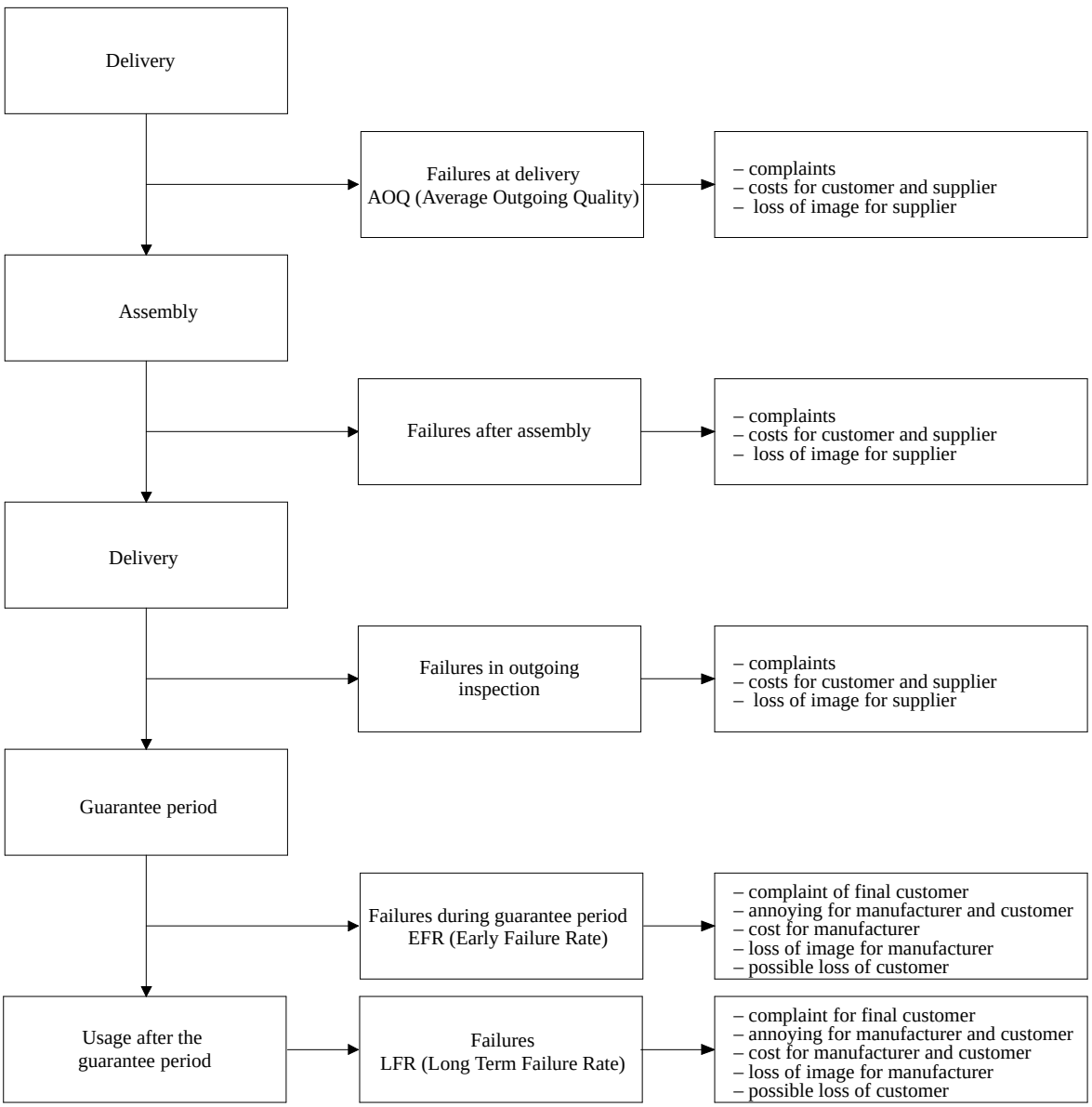


Figure 14. Possibilities of failures during life of a semiconductor component

In principle, this sequence is valid for all components of a product.

This clearly shows the negative consequences of a failure which become more serious and expensive the later they occur. The manufacturer is therefore interested in supplying products with the lowest possible

- AOQ (Average Outgoing Quality) value
- EFR (Early Failure Rate) value
- LFR (Long-term Failure Rate) value

Average Outgoing Quality (AOQ)

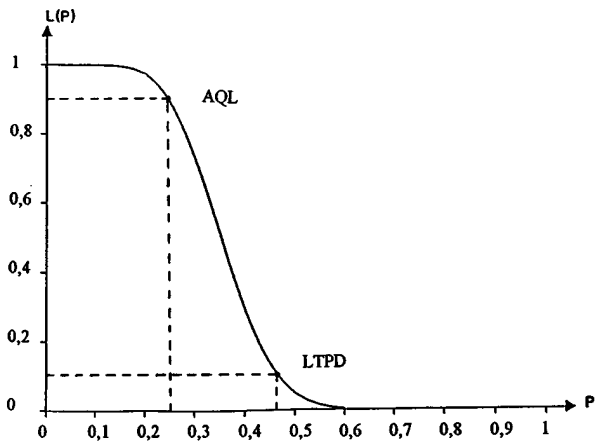


Figure 15. OC-function

L(P) Acceptance probability

P Failure rate of one lot

The AOQ is normally expressed in ppm (parts per million) and represents the average number of failed parts in deliveries over a period of time, i.e., the delivered quality. The AOQ value is determined by outgoing sample inspection by the supplier or incoming sample inspection by the customer. As a rule, the sample inspection is based on AQL- or LTPD tables.

The connection between the acceptance probability of one lot and the failure rate is given by the Operating Characteristic (OC, see figure 15).

In using AQL-values, the supplier's risk is defined. A lot with a permissible failure ($p < p_{limit}$) will not be delivered with an error probability of 10%.

In using LTPD-tables, the facts are vice versa. With an error probability of 10% a lot will not be accepted with a permissible failure rate ($p > p_{limit}$). Usually this risk is also called the buyer's risk. The LTPD as opposed to the AQL is independent from the size of the used lot. The selectivity increases with increasing sample size, i.e., AQL and LTPD come closer. The amount of the OC curve's gradient increases. Ideally (gradient = $-\infty$; sample size equals lot size, $n \rightarrow N$) the values of AQL and LTPD are equal.

Customer and supplier should agree which of the tables should be used. If necessary they can be taken from the basic information on statistical quality assurance. The following two tables include all necessary data like lot size, sample size, number of failures allowed and corresponding AQL or LTPD values related to a given confidence level.

Table 1. LTPD-table for 90% confidence level

LTPD	50	30	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3	0.2	0.15
Number of failures to accept lot	Minimum size of sample															
0	5	8	11	15	22	32	45	76	116	153	231	328	461	767	1152	1534
1	8	13	18	25	38	55	77	129	195	258	390	555	778	1296	1946	2592
2	11	18	25	34	52	75	105	176	266	354	533	759	1065	1773	2662	3547
3	13	22	32	43	63	94	132	221	333	444	668	953	1337	2226	3341	4452
4	16	27	38	52	78	113	158	265	398	531	798	1140	1599	2663	3997	5327
5	19	31	45	60	91	131	184	308	462	617	927	1323	1855	2663	3997	5327

Table 2. AQL table, AEG 1415

normal inspection	AQL											reduced inspection
	0.06	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5	
N	n–c (D_{max} in %)											N
2–15	200–0 (0.18)	125–0 (0.29)	80–0 (0.45)	50–0 (0.71)	32–0 (1.1)	20–0 (1.7)	13–0 (2.6)	8–0 (3.9)	5–0 (6.7)	3–0 (9.6)	2–0 (15.6)	2–15
16–50										13–1 (4.8)	8–1 (9.2)	16–150
51–150								32–1 (2.3)	20–1 (3.6)	20–2 (6.0)	20–3 (8.4)	151–280
151–280							50–1 (1.5)		32–2 (3.8)	32–3 (5.4)	32–5 (8.8)	281–500
281–500						80–1 (1.0)		50–2 (2.4)	50–3 (3.5)	50–5 (5.7)	50–7 (8.1)	501–1200
501–1200					125–1 (0.64)		80–2 (1.6)	80–3 (2.2)	80–5 (3.7)	80–7 (5.2)	80–10 (7.7)	1201–3200
1201–3200				200–1 (0.41)		125–2 (1.1)	125–3 (1.5)	125–5 (2.4)	125–7 (3.5)	125–10 (5.0)	125–14 (7.2)	3201–10000
2101–10000			315–1 (0.27)		200–2 (0.68)	200–3 (0.68)	200–5 (1.6)	200–7 (2.2)	200–10 (3.2)	200–14 (4.6)	200–21 (7.3)	10001–35000 [1]
10001–35000		500–1 (0.17)		315–2 (0.44)	315–3 (0.61)	315–5 (0.99)	315–7 (1.4)	315–10 (2.1)	315–14 (3.0)	315–21 (4.7)		

[1] Lots over about 35,000 must be divided

Early Failure Rate (EFR)

EFR is an estimate (in ppm) of the number of early failures related to the number of devices used. Early failures are normally those which occur within the first 300 to 1000 hours. Essentially, this period of time covers the guarantee period of the finished unit. Low EFR values therefore are very important to the device user. The early life failure rate is heavily influenced by complexity. Consequently 'Designing-In Quality' in the development and design phase, as well as optimized process control during manufacturing, significantly reduces it.
Normally, the early failure rate should not be significantly higher than the random failure rate. EFR is given in ppm (parts per million).

Long-Term Failure Rate (LFR)

LFR shows the failure rate during the operational period of the devices. This period is of particular interest to the manufacturer of the final product. Based on the LFR value, estimations concerning long-term failure rate, reliability and useful life of a device or module may be derived. The useful life time is normally the period of constant failure rate. All failures occurring during this period are random.

LFR is given in FIT (Failures In Time).

One industrial sector having extreme requirements for devices and components is the automobile industry. A useful life time of 10 years with an annual rate of 20,000 km is taken for granted.

Electronic components for cars consist of many single devices which often constitute functionally a series circuit. Such circuits assume the full function of all single components. The product of the separate function probabilities is the functional probability of the complete system.

The following calculation shows:

For high functional probability of such a circuit, extremely low failure rates of the single components are required.

A car's electronic system consists of many single components/parts, all of which are independently necessary for the car's full function. All of these single components/ parts may independently fail with a specified probability.

Single system

Probability of a single component to fail

$$p = 0.001 \ (0.1\%)$$

Probability of a single component not to fail

$$q = 1 - p = 0.999 \ (99.9\%)$$

For the sake of simplicity we assume that a system consists of many single components/ devices, which all fail with the same probability. The function of all subsystems is necessary for the function of the main system.

As an example, a main system consists of 100 single components/ parts. The single probabilities that the single components/ parts do not fail are:

Probability (A_1 does not fail) = q_1;
Probability (A_2 does not fail) = q_2;
.
.
.
Probability (A_n does not fail) = q_n;

The probability that the main system does not fail (that means, neither subsystem A1, A2 ... nor subsystem An fails) is wanted. This equals the function of all subsystems. The probability that the main system will fail is the complement of the above.

Complete system

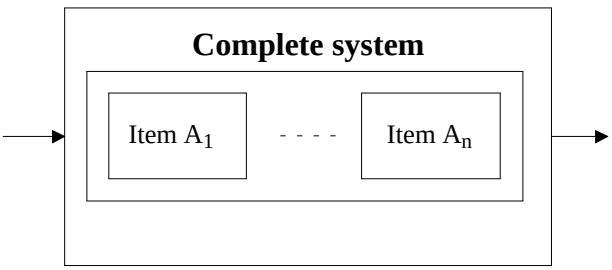


Figure 16. Complete system

Probability of the complete system to fail (complement of 1):

$$q_{tot} = 1 - q_{ges}$$

Probability of the complete system not to fail:

$$q_{tot} = q_1 \times q_2 \times ... \ q_n$$

This results for a main system such as the example:

$$q_{tot} = 0.999^{100} = 0.9$$
$$p_{tot} = 1 - 0.9 = 0.1$$

This means, that a main system which consists of 100 subsystems, each with a probability of 0.1% to fail, will only work with statistical average probability of 90%. Expressed vice versa, such a system will fail with a probability of 10%.

The manufacturer of a car must promise the customer a guarantee period of cost-free repair. In order to estimate the risk of a complaint, the manufacturer needs data about the assurance of function, i.e., the reliability of the devices. Normally these may be obtained from the manufacturer of the semiconductor components.

In addition, the purchaser of a car expects no repairs, except for parts subject to wear and tear, within a minimum of 10 years.

With respect to the electronic components, this means an operational period in excess of 10,000 hours (depending upon application and use in the car) without failure, often under extreme environmental conditions, e.g., high/ low temperature is expected.

Accelerated testing is needed for assurance of these long operation periods and for determination of reliability data. Specific test procedures (see table 3) allow accelerated simulation of different operational loads. These short but nevertheless useful test procedures are becoming increasingly important.

Table 3. Accelerating load for different types of failure

Type of Failure	Accelerating Load
Intermetallic connections	Temperature
Die crack	Thermal shock
Interrupted metal layers at oxide layers	Current density /thermal shock
Bond adhesion	Thermal shock
Lifted/ not adhering metallisation	Thermal shock
Oxide defects	Temperature/ voltage
Corrosion	Humidity/ temperature
Electro-migration	Current density/ temperature

Failure Rates for Semiconductors

Models and methods have been developed which are commonly recognized and used in many cases as fundamentals for the calculation of reliability data and failure rates.

Generally the failure rate is:

$$\lambda\ (t) = -\frac{1}{R(t)} \times \frac{dR(t)}{dt}$$

R(t) is the probability of survival.

The failure rate during the operational period is normally constant, i.e., dependent on time.

In order to get information about life time, tests are performed with samples from production parts. The most important test for reliability data is the electrical life test. It simulates the dynamic operation of the device at higher temperature. The measure for reliability is the number of failures within a stipulated period or the time to failure. The most important characteristic is the life time, T. The time parameter, t, is a random number which may normally be represented by the Weibull distribution.

t Time parameter
(e.g., operation time, driving distance etc.)
$0 \leq t \leq \infty$

T Characteristic life time
(range parameter)
$T > 0$

b Gradient of failure
(form parameter)
$b > 0$

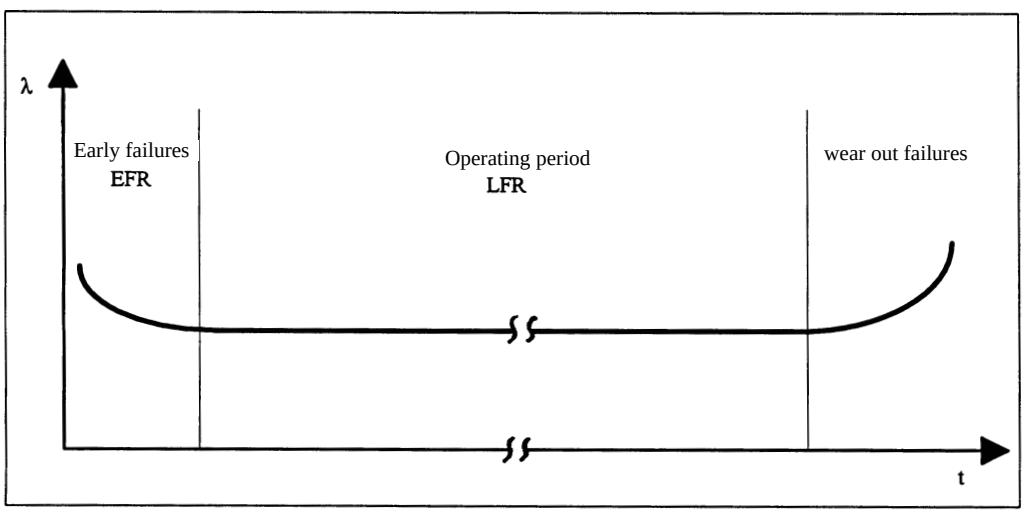


Figure 17. Bath tub curve

The life time distribution, which is characterized by the bath tub curve, may be divided into three different areas (see figure 17). The Weibull distribution may be fitted to the failure rate curve, i.e., the different periods of time (period of early failures, operation period, period subject to wear and tear).

Parameter, b, determines the distribution's form and matches it with the failure behavior. Depending on the failure gradient, b, the Weibull distribution approximates to other, simpler life time distributions, such as:

$b = 1$	Exponential distribution (single failures occur randomly)
$1.5 \leq b \leq 3$	Lognormal distribution
$b = 2$	Rayleigh distribution
$3.1 \leq b \leq 3.6$	Normal distribution

For semiconductors, the following is normally valid:

- The early failure rate is weak distinctive. This area is improved by 'Designing-In' of quality during the design/ development phase.
- The wearout phase is not reached. This must be assured by the user.
- There is no dominant failure mechanism. The activation energy used for bipolar technologies is 0.7 eV.
- The failure mechanism corresponds to a Poisson process (seldom events).

If all of these presumptions are true, the exponential distribution (Weibull distribution with $b = 1$) may be used for life time estimation.

$$f(t) = \lambda \times e^{-\lambda t}$$

Here, "λ" is constant for the operation period. The failure rate λ in this case is:

$$\lambda = \frac{r}{\sum(\text{Quantity} \times \text{Time to Failure})} \times \left[\text{hours}^{-1}\right]$$

r: number of failures

The measure of λ is FIT (Failures In Time = number of failures in 10^9 device hours)

Example

A sample of 500 semiconductor devices is tested in a operating life test (dynamic electric operation). The devices operate for a period of 10,000 hours.

Failures: 1 failure after 1000 h
1 failure after 2000 h

The failure rate may be calculated from this sample by

$$\hat{\lambda} = \frac{2}{1 \times 1,000 + 1 \times 2,000 + 498 \times 10,000}$$

$$= \frac{2}{4,983,000} = 4.01 \times 10^{-7} \ [\text{hours}^{-1}]$$

This is a $\hat{\lambda}$-value of 400 FIT, i.e., this sample on average has a failure rate of 0.04%/1000 h.

Confidence Level

The failure rate, $\hat{\lambda}$, calculated from the sample, is an estimate of the unknown failure rate λ of the lot.

The interval of the failure rate (confidence interval) may be calculated dependent upon confidence level and sample size.

The following is valid:

- The larger the sample size, the narrower the confidence interval.
- The lower the confidence level of the statement, the narrower the confidence interval.

The confidence level applicable to the failure rate of the whole lot when using the estimated value of $\hat{\lambda}$ is derived from the χ^2-distribution. In practice, only the upper limit of the confidence interval (the maximum average failure rate) is used.

Table 4. $\chi^2/2$

Number of Failures	Confidence Level			
	50%	60%	90%	95%
0	0.60	0.93	2.31	2.96
1	1.68	2.00	3.89	4.67
2	2.67	3.08	5.30	6.21
3	3.67	4.17	6.70	7.69
4	4.67	5.24	8.00	9.09
5	5.67	6.25	9.25	10.42
6	6.67	7.27	10.55	11.76
7	7.67	8.33	11.75	13.16
8	8.67	9.35	13.00	14.30
9	9.67	10.42	14.20	15.63
10	10.67	11.42	15.40	16.95

It follows therefore:

$$\lambda_{max} = \frac{\chi^2/2\ (r;\ P_A)}{n \times t} \text{ in } [\text{hours}^{-1}]$$

$$LFR = \frac{\chi^2/2\ \ (r;\ P_A)}{n \times t} \times 1 \times 10^9 \text{ in } [\text{FIT}]$$

r: Number of failures
P_A: Confidence level
n: Sample size
t: Time in hours
$n \times t$: Device hours

The $\chi^2/2$ for λ are taken from table 4.

For the above example

from table 4:
$\chi^2/2$
$(r = 2; P_A = 60\%) = 3.08$, $n \times t = 4{,}983{,}00$ hours

$$\lambda_{max} = \frac{3.08}{4,983,000} = 6.18^{-7} [\text{hours}^{-1}]$$

This means, that the failure rate of the lot does not exceed 0.0618%/1000 h (618 FIT) with a probability of 60%.

If a confidence level of 90% is chosen from the table 3.2:
$\chi^2/2\ (r = 2; P_A = 90\%) = 5.3$

$$\lambda_{max} = \frac{5.3}{4,983,000\ \text{h}} = 1.06^{-6}\ [\text{hours}^{-1}]$$

This means, that the failure rate of the lot does not exceed 0.106%/1000 h (1060 FIT) with a probability of 90%.

In practise, the number of devices used – as well as the test time – is lower than in the given example.

Operating Life Tests

Number of devices tested: n = 50

Number of failures (positive qualification): c = 0

Test time: = 2000 hours

Confidence level: $P_A = 60\%$

$\chi^2/2$ (0; 60%): 0.93

$$\lambda_{max} = \frac{0.93}{50 \times 2,000} = \frac{0.93}{100,000} = 9.3^{-6}\ [\text{hours}^{-1}]$$

This means, that the failure rate of the lot does not exceed 0.93%/1000 h (9300 FIT) with a probability of 60%.

This example demonstrates that it is only possible to verify LFR values of 9300 FIT with a confidence level of 60% in a normal qualification tests (50 devices, 2000 h).

To obtain LFR values which meet today's requirements (< 50 FIT), the following conditions have to be fulfilled:

- Very long test periods
- Large quantities of devices
- Accelerated testing (e.g., higher temperature)

In order to verify LFR-values in the range of 40 FIT with a confidence level of 60%, the number of device hours necessary is:

$$n \times t = \frac{0.93}{40} \times 1 \times 10^9 = 23,250,000 = 2.3 \times 10^7$$

If a confidence level of 90% is required,

$$n \times t = \frac{2.31}{40} \times 1 \times 10^9 = 57,750,000 = 5.7 \times 10^7$$

device hours are needed for verification.

It is impossible to obtain these extremely high number of device hours during qualification testing. Therefore, an additional monitoring system has been implemented. With this monitoring system, very high numbers of devices are tested. This serves on the one hand to obtain a data base for reliability information, and on the other hand to provide continuous monitoring of production.

Feedback from Customers

The verification of very low ppm and FIT values requires very high numbers of tested devices, i.e., very high numbers of device hours in stress. For reasons of time and costs, the performance of these tests is only possible on a limited sample. The supplier therefore needs data from customers in addition to data from his own tests.

The supplier can evaluate the effectiveness of his test methods from customer data. Customer feedback is therefore very important to the supplier in order to optimize his test procedures.

Feedback should contain the following data:

- Failure rates of customer's incoming inspection, related to device types and amount delivered
- Failure rates of customer's assembly with exact information of time to failure , related to device type and number of parts built in
- Failure rates in the field, related to device types, with data on operation conditions and operation time as exact as possible

If a manufacturer of semiconductors gets data regularly, he can correlate practice with performed tests. This allows the supplier to optimize his production and test methods.

Mean Time To Failure (MTTF)

For systems which can not be repaired and whose devices must be changed, i.e., as semiconductors, then:

$$MTTF = \frac{1}{\lambda}$$

MTTF is the average fault-free operating period per a monitored (time) unit.

If you use an exponential life time distribution

$$f(t) = \lambda \times e^{-\lambda t}$$

and put in t = MTTF = $1/\lambda$, you get:

$$f\left(\frac{1}{\lambda}\right) = \lambda \times e^{-\lambda\frac{1}{\lambda}}$$

$$f\left(\frac{1}{\lambda}\right) = \lambda \times e^{-1}$$

$$f\left(\frac{1}{\lambda}\right) = \lambda \times 0,367$$

Only 36.7% of the devices 'survive' time t = MTTF.

As stated before, semiconductors have an exponential life time distribution. This corresponds to the statement that only 36.7% of the initial devices still work after time t = MTTF.

From this, it is possible to calculate the maximum allowed MTTF for a defined percentage of devices to be working after a specified period of time.

Example

90% of devices in a system should still operate after 10 years. This equals the statement that 10% of the devices may fail within 10 years.

$$f(t) = \lambda \times e^{-\lambda t}$$

$$F(t) = \lambda \times \int_0^t e^{-\lambda t}\, d\tau = 1 - e^{-\lambda t}$$

$$\Rightarrow 1\text{–}F(t) = e^{-\lambda t}$$

$$\Rightarrow \ln\,[1\text{–}F(t)] = -\lambda \times t$$

$$\Rightarrow \lambda = \frac{-\ln\,[1\text{–}F(t)]}{t}$$

$$\Rightarrow MTTF = \frac{1}{\lambda} = \frac{t}{-\ln\,[1\text{–}F(t)]}$$

With F(t) = 0.1 and t = 10 years = 87,600 hours results:

$$\lambda = \frac{-\ln\,[1\text{–}F(t)]}{t} = \frac{-\ln\,(1\text{–}0.1)}{87,600\ h} = 1.2 \times 10^{-6}$$

$$MTTF = \frac{1}{\lambda} = \frac{t}{-\ln\,[1\text{–}F(t)]} = \frac{10\ years}{-\ln\,(1\text{–}0.1)}$$

$$\approx 95\ years$$

This applies to a single system. In a complex system, the failure rates of all components which may fail independently and which are necessary for the function of the complete system must be considered.

Mean Time Between Failure (MTBF)

In comparison, MTBF is defined for units which may be repaired (i.e., modules) as the average failure interval.

Probability of Survival

The ‘probability of survival’ is defined as the probability that a unit (device) may survive a defined time period.

Accelerating Stress Tests

Innovation cycles in the field of semiconductors are getting shorter and shorter. This means that products must be brought to the market quicker. At the same time, expectations concerning the quality and reliability of the products have become higher.

Manufacturers of semiconductors must therefore assure long operation periods with high reliability but in a short time. Sample stress testing is the most commonly used way of assuring this.

Tests are performed at high environmental temperatures in order to accelerate the time to failure (see table 3) because most failure mechanism of semiconductors are dependent upon temperature.

The rule of Arrhenius describes this temperature dependent change of the failure rate.

$$\lambda(T_2) = \lambda(T_1) \times e^{\left[\frac{E_A}{k} \times \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]}$$

Boltzmann’s constant
$k = 8.63 \times 10^{-5}$ eV/K

Activation energy
E_A in eV

Junction temperature real operation
T_1 in Kelvin

Junction temperature stress test
T_2 in Kelvin

Failure rate real operation
$\lambda\,(T_1)$

Failure rate stress test
$\lambda\,(T_2)$

The acceleration factor is described by the exponential function to be:

$$AF = \frac{\lambda(T_2)}{\lambda(T_1)} = e^{\left[\frac{E_A}{k} \times \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]}$$

Example

The following conditions apply to an operating life stress test:

Environmental temperature during stress test
$T_A = 125°C$

Power dissipation of the device
$P_V = 250$ mW

Thermal resistance junction/environment
$R_{thJA} = 100$ K/W

The system temperature/ junction temperature results from:

$T_J = T_A + R_{thJA} \times P_V$

$T_J = (125 + 100 \times 0.25)^oC$

$T_J = 150^oC$

Operation in the field at an ambient temperature of 100°C and at an average power dissipation of 100 mW is utilized. This results in a junction temperature in operation of T_J = 110°C. The activation energy used for bipolar technologies is E_A = 0.7 eV.

The resulting acceleration factor is:

$$AF = \frac{\lambda(423)}{\lambda(383)} = e^{\left[\frac{E_A}{k} \times \left(\frac{1}{383} - \frac{1}{423}\right)\right]}$$

$AF \approx 7.4$

This signifies that, regarding this example, the failure rate is lower by a factor of 7.4 compared to the stress test.

Other accelerating stress tests may be:

- HAST (High Accelerated Stress Test)
  T_A = 130°C,
  Relative Humidity (RH) = 85%
- Humidity
  T_A = 85°C
  RH = 85%
- Temperature cycling
  Temperature interval as specified

The tests are carried out according to the requirements of appropriate IEC-standards (see also chapter ‘Qualification and Release’).

Activation Energy

There are some conditions which need to be fulfilled in order to use Arrhenius’ method:

- The validity of Arrhenius’ rule has to be verified.
- ‘Failure-specific’ activation energies must be determined.

These conditions may be verified by a series of tests. Today, this procedure is generally accepted and used as a basis for estimating operating life. The values of activation energies can be determined by experiment for different failure mechanisms.

Example

Crystal effects	1.0 to 1.5 eV
Electro-migration	0.5 to 0.9 eV
Oxide failures	0.3 to 0.5 eV
Humidity effects	0.5 to 0.9 eV

Values often used for different device groups are:

Opto components	0.7 eV
Bipolar ICs	0.7 eV
MOS ICs	0.6 eV
Transistors	0.7 eV
Diodes	0.7 eV

Using this method, it is possible to provide long-term predictions for the actual operation of semiconductors even with relatively short test periods.

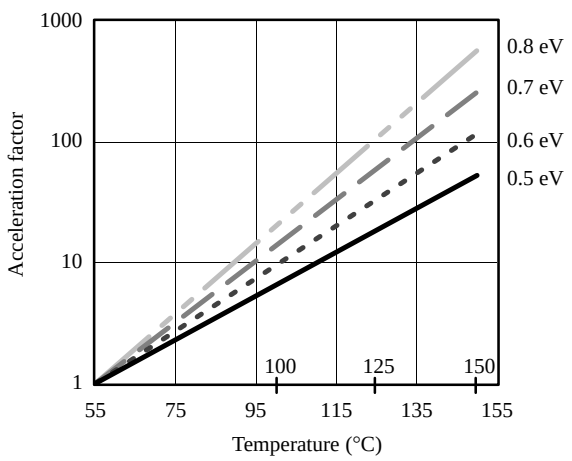


Figure 18. Acceleration factor for different activation energies normalized to T_J = 55°C

Electrostatic Discharge

The rapid progress in semiconductors has resulted in

- Smaller structures
- Reduced power consumption
- Higher complexity
- Higher speed

At the same time this has resulted in an increased susceptibility to Electrostatic Discharge (ESD).

Definition

ESD is the high voltage which is generated when two dissimilar materials move in contact with one another. This may be rubbing (i.e., walking on carpet) or hot air or gas passing over an insulated object. Sometimes, these are easily detectable as when a person is discharged to ground (shock).

Electronic devices may be irreversibly damaged when subjected to this discharge. They can also be damaged if they are charged to a high voltage and then discharged to ground.

This damage from ESD may occur at any point in the process of manufacture and use of the device. It is a particular problem if the humidity is low (< 40%) which is very common in non-humidified but air-conditioned buildings. It is not just generated by the human body but can also occur with ungrounded machinery.

The ESD discharge may cause a device to fail immediately or damage a device so that it will fail later. Whether this happens is usually a function of the energy available in the ESD pulse.

Protection against ESD

There are various ways in which semiconductor devices may be protected from damage by ESD.

- Use of protection structures on chip to discharge the ESD
- Use of ESD preventative measures during handling
- Use of ESD protection measures during handling
- Use of application-specific circuitry

Protection Structures

There are many techniques used on chip to provide protection against ESD. These techniques have improved in-line with semiconductor technology. They have improved particularly in terms of speed of operation and the energy which they can handle.

They all have certain characteristics in common.

- They must not influence device performance
- They must not significantly alter input/ output characteristics
- They must be faster than the circuitry which they protect
- They must protect in both directions
- They must protect in both the charge and discharge mode

Unfortunately, there is no perfect protection structure which will protect all types of devices under all conditions. For this reason, both ESD protective and preventative measures are essential.

ESD Prevention

All means possible must be taken to prevent the generation of static electricity. Telefunken Semiconductors' procedures for this are detailed in their internal document QSA 3006. These requirements meet or exceed those of CECC 00015, the European Standard for semiconductor protective and preventative measures. These include the use of:

- Earthed wriststraps
- Earthed benches
- Conductive floors

- Protective clothing
- Controlled humidity

It also lays down the methods for routinely checking these and other items such as the earthing of machines. Materials suitable for use in ESD-controlled environments are detailed.

ESD Protection

A semiconductor device is only completely protected when enclosed in a “Faraday Cage”. This is a completely closed conductive container (i.e., sealed conductive bag or box).

Most packaging material (i.e., tubes) used for semiconductors is now manufactured from antistatic material or antistatic coated material. This does not mean that the devices are completely protected against ESD, merely that the packing will not generate ESD. Devices are only completely protected when encased in a conductive container.

It should also be remembered that devices can equally as easily be damaged by discharge from a high voltage to ground as vice-versa.

Application-Specific Protection

Though more difficult, devices can still be damaged once in circuit. This may be from ESD during board handling but may also be from application-related conditions. Typical of this is flash-over in TV sets and high voltage inductively-produced spikes in automotive applications. In these cases, it may be necessary to add application-specific circuitry. This usually consists of the use of capacitors or zener diodes added external to the device itself.

Tests

ESD may emerge from a variety of sources both human and machine generated. It may be both from the charging or the discharging of the body in question. For the purposes of testing devices, several models have been proposed. These may be split into three groups:

- Human Body Model (HBM)
- Machine Model (MM)
- Charged Device Model (CDM)

Human Body Model (HBM)

This model simulates the discharge of a charged human body through a device. It uses the discharge of a 100 pF capacitor through a 1.5 kΩ resistor. The actual set up normally corresponds to one of the international standards. Telefunken Semiconductors utilizes MIL-STD-883 Method 3015.7.

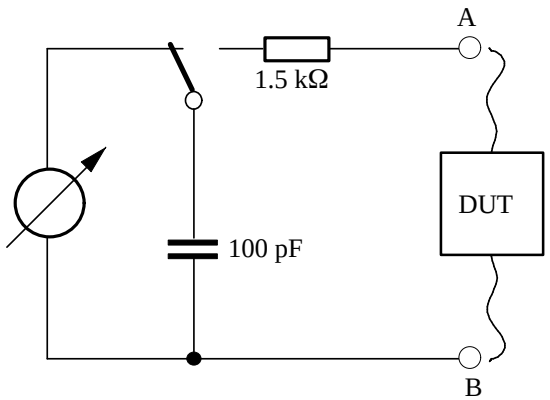


Figure 19. Human Body Model

Machine Model (MM)

This model simulates the discharge of a charged machine through the device. It uses the discharge of a 200 pF capacitor through a 0 Ω resistance. The test procedure is similar to the HBM but it is not so well-defined internationally. The EOS/ESD test defines the waveforms and is becoming the standard for this test.

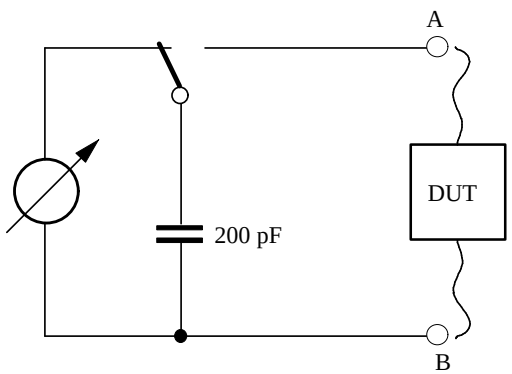


Figure 20. Machine Model

Charged Device Model (CDM)

This model simulates the discharge of a charged device to ground. In this test, the device is charged to a known voltage and discharged to ground through 0 Ω. The EOS/ ESD specification has a proposal for a standard but this is as yet only a proposal. Two extensions to this model are proposed:

- Contact mode – discharged by contact
- Non-contact mode – discharged by proximity to a grounded object

Test Equipment

In order to have comparative results about devices, they must be measured on the same test equipment (manufacturer/ model). Different testers though supposedly testing to the same model can supply completely different current waveforms. This is mainly a function of parasitics (capacitance, inductance etc). The most important factor when comparing tests and equipment is the discharge waveform.

Test Procedure

It is worth noting that there is normally a difference in the procedures for qualification and evaluation. For qualification, only a limited series of tests is conducted. This may be limited to certain combinations of pins (i.e., all supply pins in parallel) and devices are only tested at one voltage to make certain that they will function after that voltage has been applied.

For evaluation, it is usual to look at all combinations of pins and to measure the highest voltage which will not cause the device to fail.

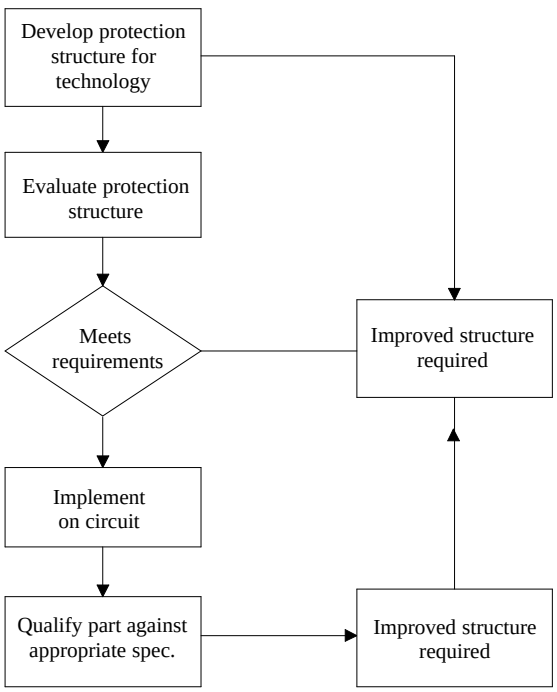


Figure 21. Procedure qualification tests

Responsibility

Both Telefunken Semiconductors and its customers have responsibilities with respect to ESD protection. These are:

Telefunken Semiconductors has certain responsibilities with respect to protection against ESD and the testing for ESD hardness. These may be in four parts:

- The design, development and improvement of structures for ESD protection
- The qualification of the structures used in its products
- The testing of the products to ensure adequate ESD protection
- The use of ESD prevention and protection measures

The customer must also take precautions so that damage from ESD cannot occur.

- He must have an adequately ESD-protected facility and have personnel who are trained and aware of the problems of ESD
- Where there is a high risk of voltage over-stress conditions including ESD, he must provide on-board application-specific protection

Ship-to-Stock

In the framework of partnership between our customers and Telefunken Semiconductors, Ship-to-Stock (STS) delivery may be agreed in single events for “high-volume”-products.

STS-delivery means delivery of goods to the customer, where the customer performs reduced or no incoming inspection. In doing so, the customer abandons the immediate recognition of possible failures and their immediate blame (§§377, 378 HGB). This juridical designation may be omitted by mutual agreement.

By omitting §§377, 378 HGB is in agreement with the liability insurance of Telefunken Semiconductors.

The basis of each STS-delivery is a valid contract between the customer and Telefunken Semiconductors (STS-contract, Quality Assurance Agreement).

In the case of STS-deliveries, each packing unit will be sealed with a label as shown below in figure 22.

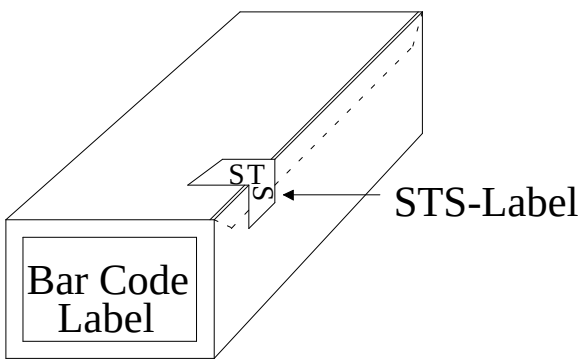


Figure 22. Sealing of the packing units

The marking “Ship-to-Stock” or “STS” contains the customer’s address. This address is printed on the outer package, the order confirmation, the packing list and the delivery sheet.

The STS label of TEMIC Heilbronn is produced as follows:

Size: ca. 5 cm $\times$ 10 cm
Color: fluorescent green

Nur mit gültigem STS-Vertrag als STS-Ware verwendbar!

S T S

Only for STS use in conjunction with valid STS contract agreement!

TEMIC–HN

Figure 23. STS-label

Definitions

AF Acceleration Factor;
see also Arrhenius' rule

AOQ Average Outgoing Quality

AQL Average Quality Level

Arrhenius
According to the rule of Arrhenius, the acceleration factor AF is calculated

Audit Internal or external revision of the system, the procedures or the products

AV Arbeitsvorschrift; working instruction

CL Confidence Level: interval which meets the unknown parameter of the lot for given assurance of statement

C_{MK} Machine Capability index

C_{PK} Process Capability index

DOE Design Of Experiments: statistical design of testing in order to optimize effort and information of test sequences

DUT Device Under Test

E_A Activation Energy: the energy which is necessary to activate semiconductor effects

EDP Electronic Data Processing

EFR Early Failure Rate

ESD ElectroStatic Discharge: electrostatic charges which may cause damage to devices

FIFO First-In-First-Out: warehouse organization principle, goods entered first will be removed first

FIT Failures In Time

FMEA Failure Mode and Effects Analysis: method of design/ development to estimate and evaluate possible failures and their consequences

ISO 9000
Explanation of fundamental terms, "Guidelines for Selection and Use" of quality management procedures and equipment

ISO 9001
Model for explaining quality assurance in design/ development/ production/ assembly and customer service

Calibration
Inspection of the standards and equipments with a direct or indirect link to the highest calibration authority, e.g., the 'Physikalisch-Technische Bundesanstalt' in Braunschweig or other approved institutions

Lambda λ
Failure rate

LFR Long-term Failure Rate

LTPD Lot Tolerance Percent Defective

Monitoring
The monitoring system is established in order to achieve fundamentals for reliability information and to monitor the on-going production

MTBF Mean Time Between Failures: determines the period between two failures for repairable systems

MTTF Mean Time To Failure: determines the period between two failures for non-repairable systems

OC Operating Characteristic: assigns the confidence level of a lot dependent from the failure percentage

OG Organization

PdA Preis der Abweichung; price of non-conformance, cost of quality

PdÜ Preis der Übereinstimmung; price of conformance, cost of quality

ppm parts per million: failure rate, related to 1,000,000 devices

PV Prüfvorschrift; test instruction

QA Quality Assurance: department which coordinates and performs Q-tasks in Front End

QFD Quality Function Deployment: a method of translating customer demands into supplier requirements

QM Quality Management

QSA Qualitätssicherungsanweisung; general quality assurance procedure

QSV Qualitätssicherungsvereinbarung; quality assurance agreement

Quality Management System
The organization, responsibilities, procedures, processes and resources needed to implement quality management

QVP Qualitätsverbesserungsprozeß; continuous quality improvement process within Telefunken Semiconductors

R&R Repeatability & Reproducibility: procedure to determine repeatability (spread of equipment) and reproducibility (spread of different operators)

SPC Statistical Process Control: serves for control of processes

STS Ship-To-Stock

TQM Total Quality Management

Waferfab
Production location for wafers (Silicon discs)

WEK Wareneingangskontrolle; incoming inspection and quality assurance for suppliers

Appendix

General Information on the Reliability Data

This section details current reliability data. The data is in sections as follows:

- AOQ-values
- EFR-values (monitoring)
- FIT-values

AOQ-values The diagrams show the development of AOQ over recent years.

EFR-values In 1994, the qualification procedure in Telefunken Semiconductors was re-structured and re-organized (see also chapter “Qualification and Release”). In the framework of this restructuring, a device monitoring system was established. Up to that time, the number of tests performed was limited. This monitoring is used in order to provide the required amount of data. The first results of these monitoring tests are shown.

FIT-values The diagrams show the development of FIT over recent years. The fundamentals for the calculation of these values are:

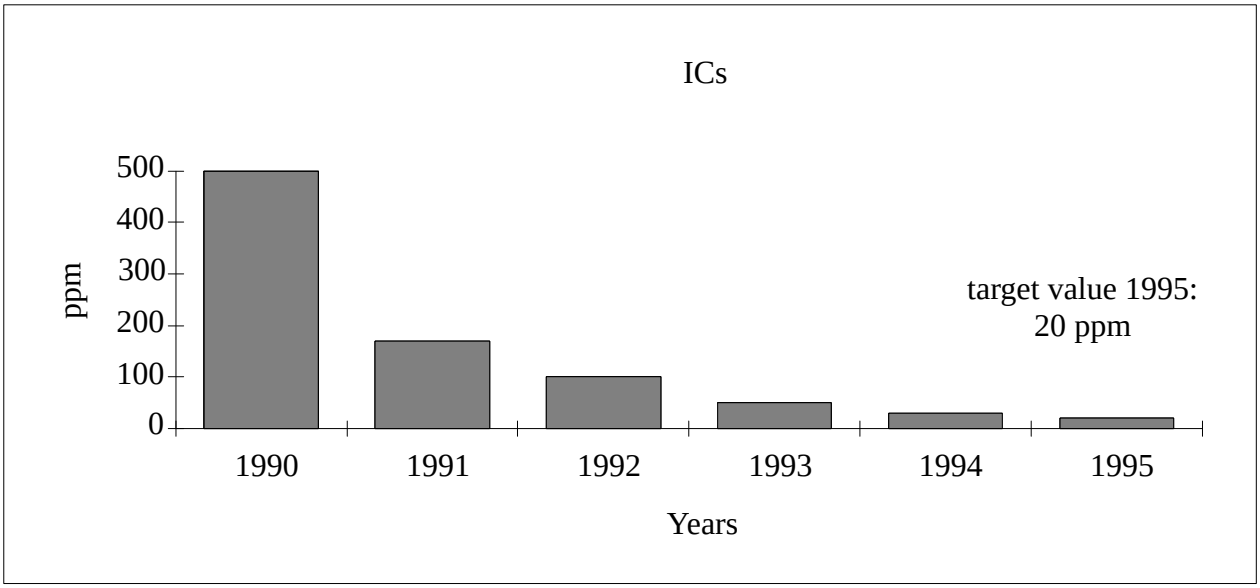
- $T_J = 55°C$
- CL = 60%
- $E_A = 0.7$ eV

The junction temperature used as a base has been chosen to be comparable with that used by competitors. Dependent upon application, devices will have different power consumption resulting in different junction temperatures (e.g., supply voltage, extent of biasing of amplifiers). The basic data given here allows the customer to easily calculate FIT-values for his own application (see chapter “Accelerating Stress Tests”).

Data is displayed according to product group.

Integrated Circuits

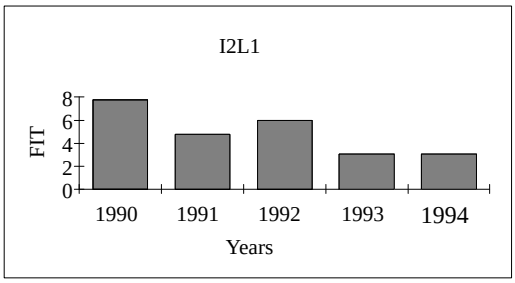
AOQ-Values ICs

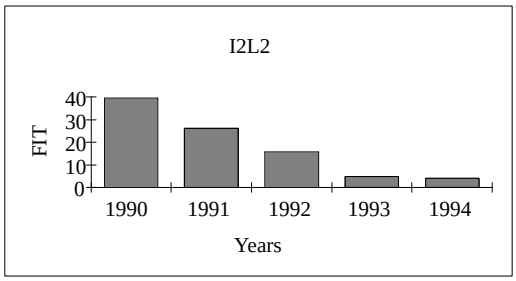


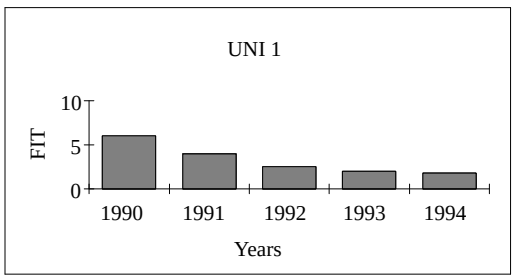
EFR-Values ICs

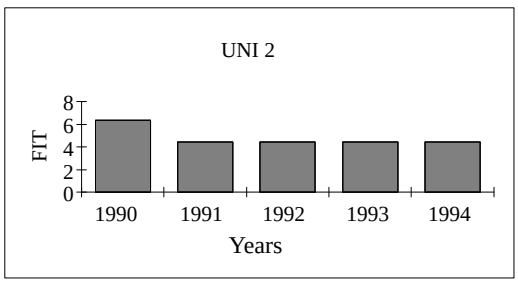
Test	Technology	Sample Size	Failures	Failure Rate in ppm
Operating life	I2L	34242	0	0
	STD 3	22653	0	0
	UNI	1240	0	0

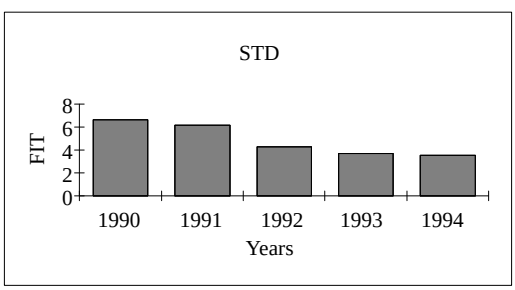
FIT-Values ICs

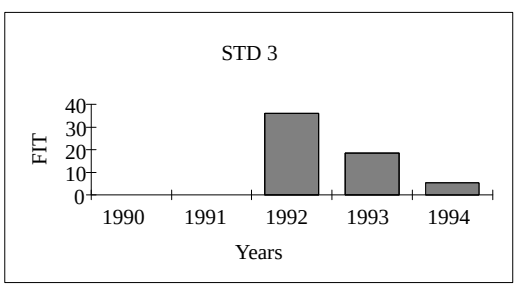


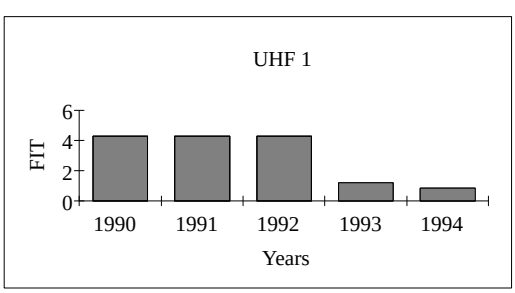


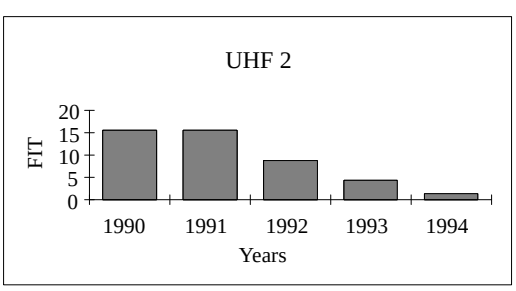


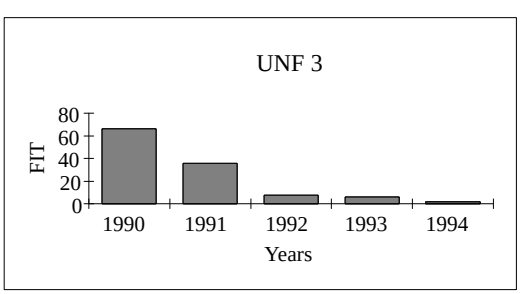


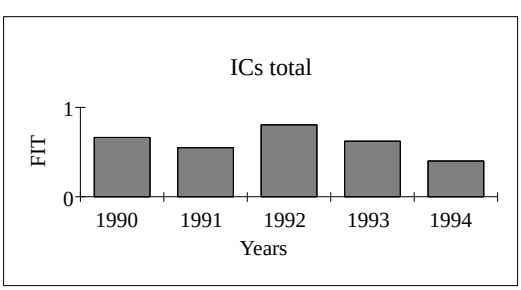






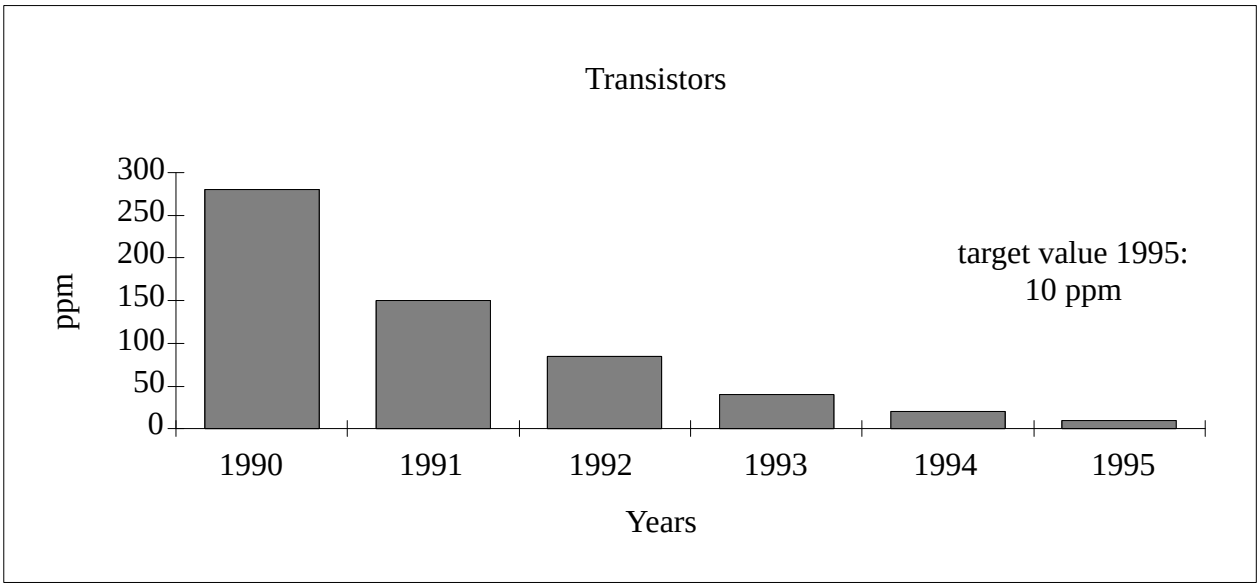






Transistors

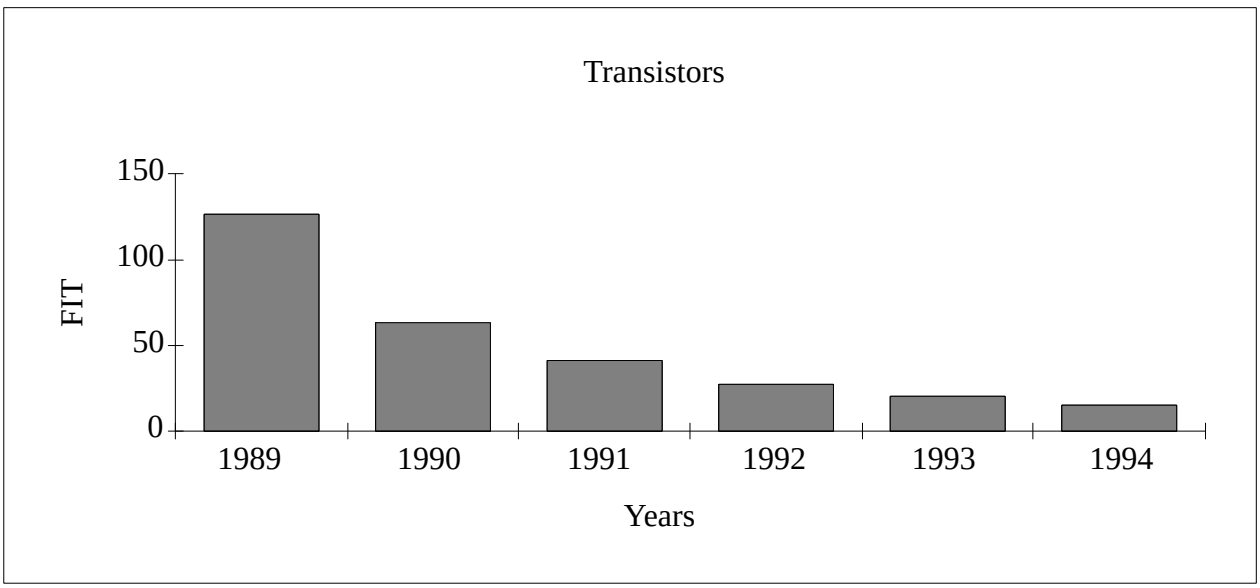
AOQ-Values Transistors



EFR-Values Transistors

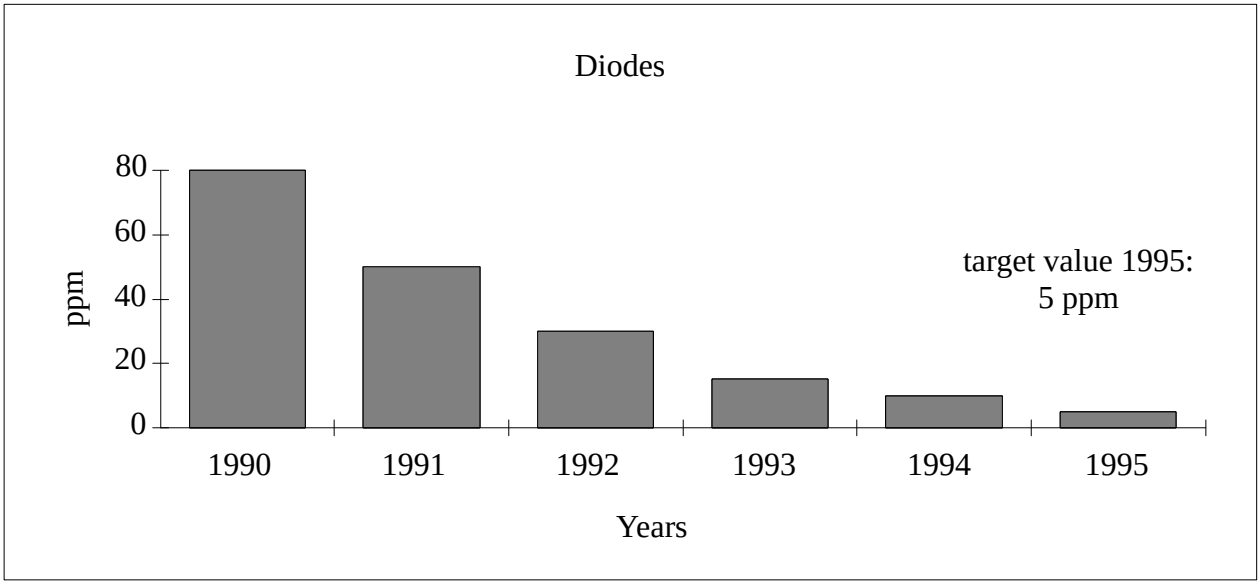
Test	Technology	Sample Size	Failures	Failure Rate in ppm
Operating life	Transistors	198	0	0

FIT-Values Transistors



Diodes

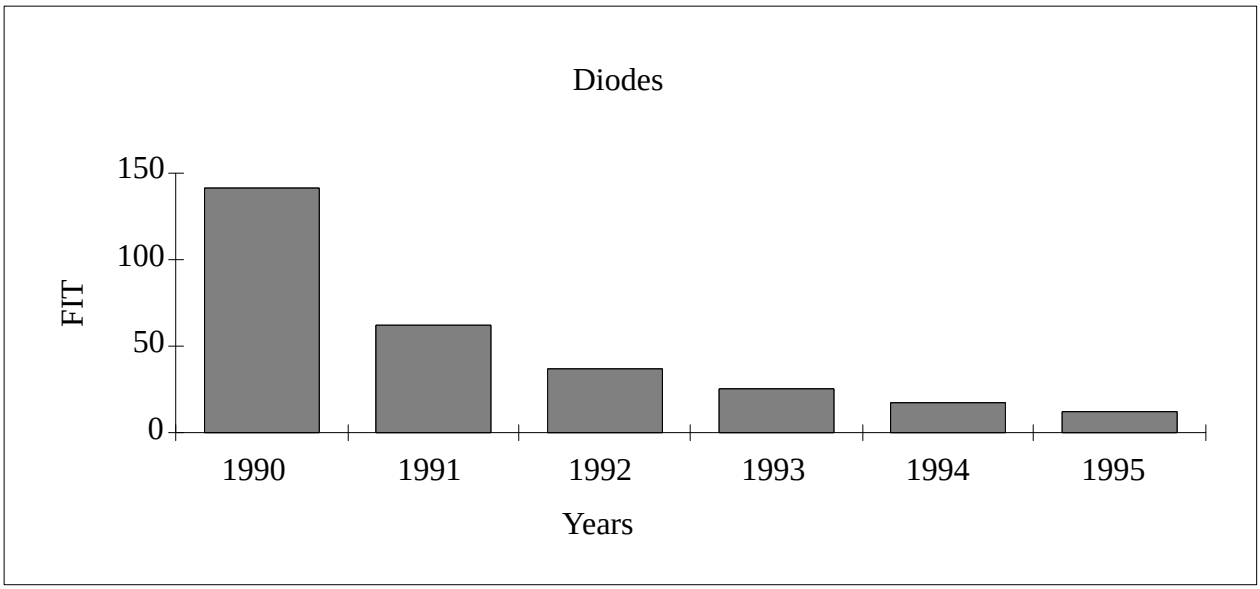
AOQ-Values Diodes



EFR-Values Diodes

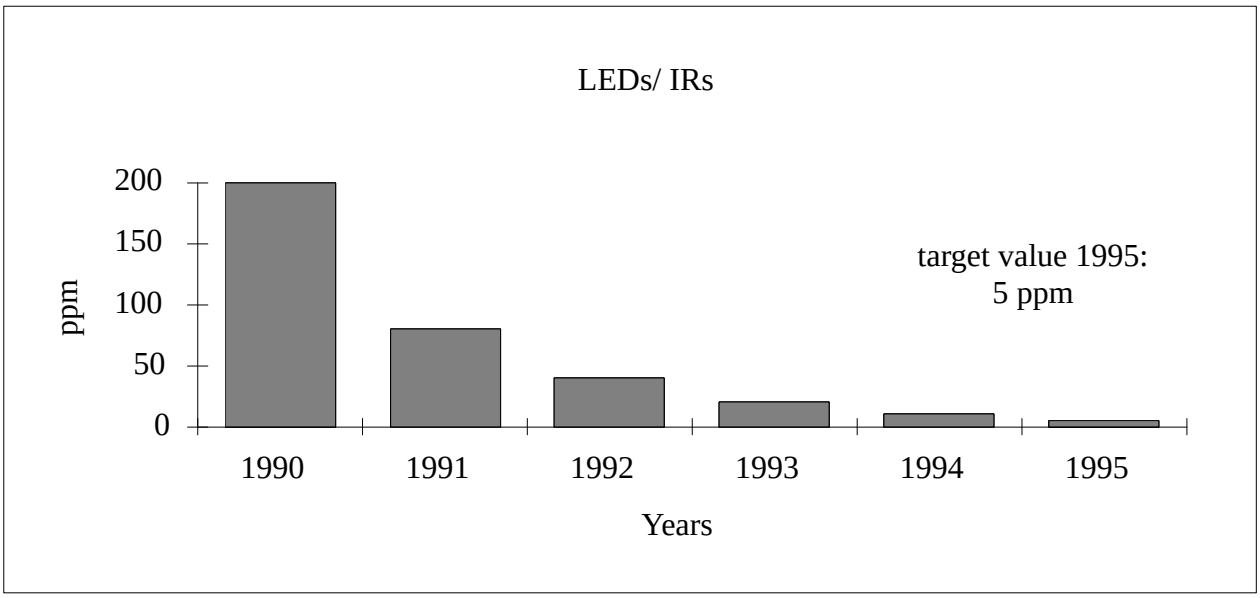
Test	Technology	Sample Size	Failures	Failure Rate in ppm
Operating life	Diodes	4900	6	1224

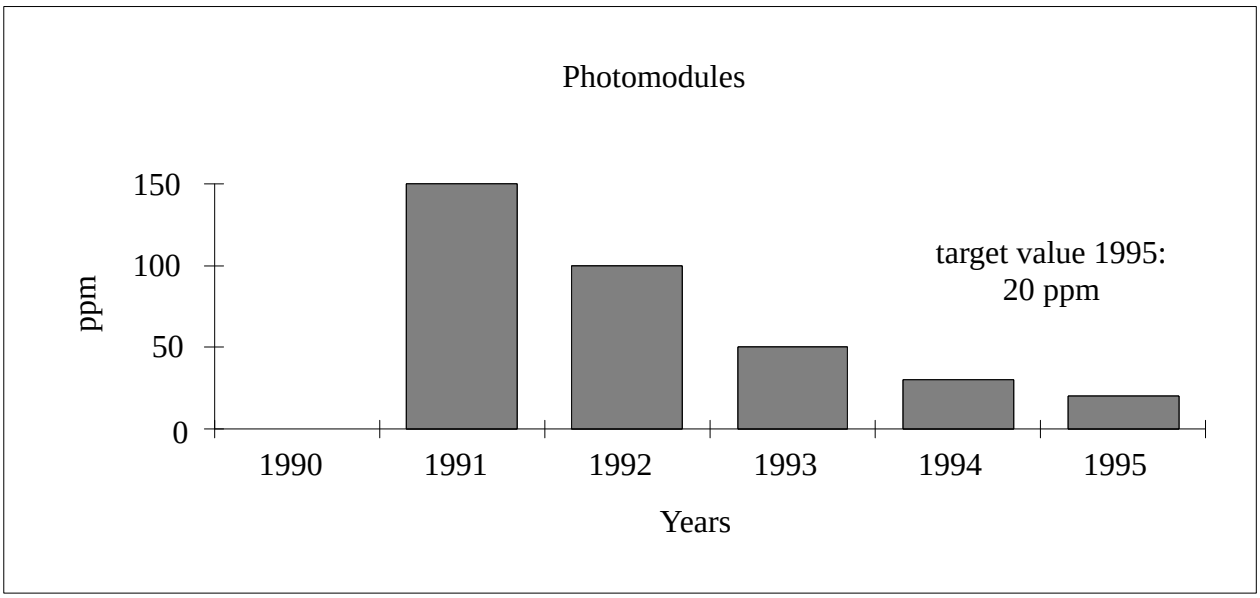
FIT-Values Diodes

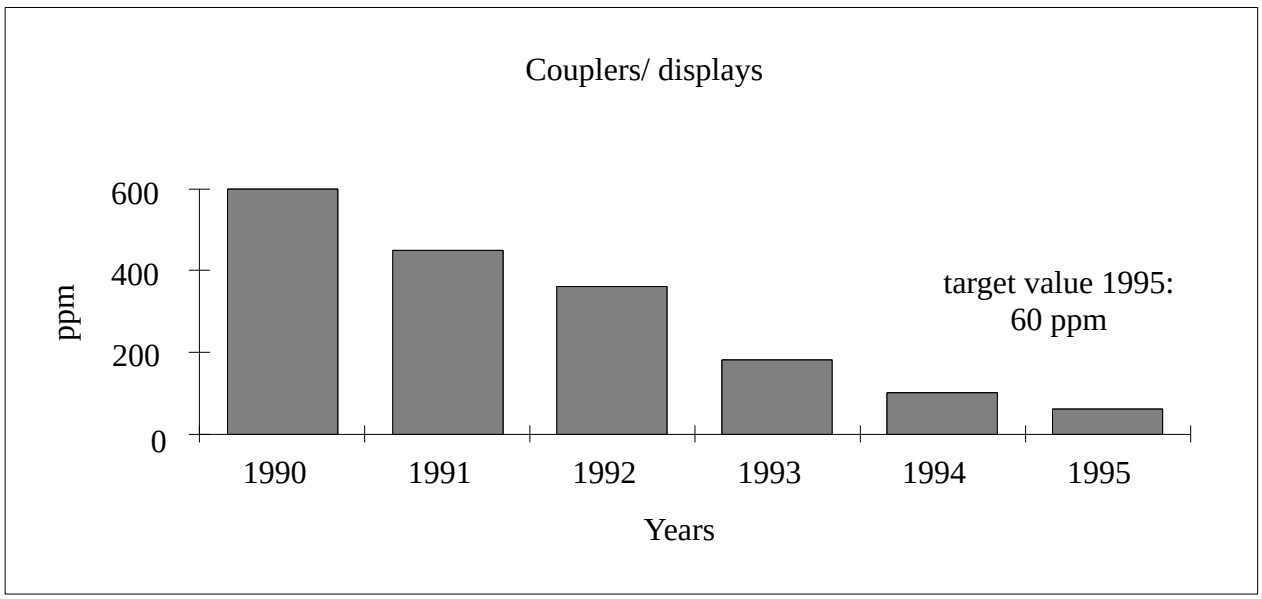


Opto Components

AOQ-Values Opto Components



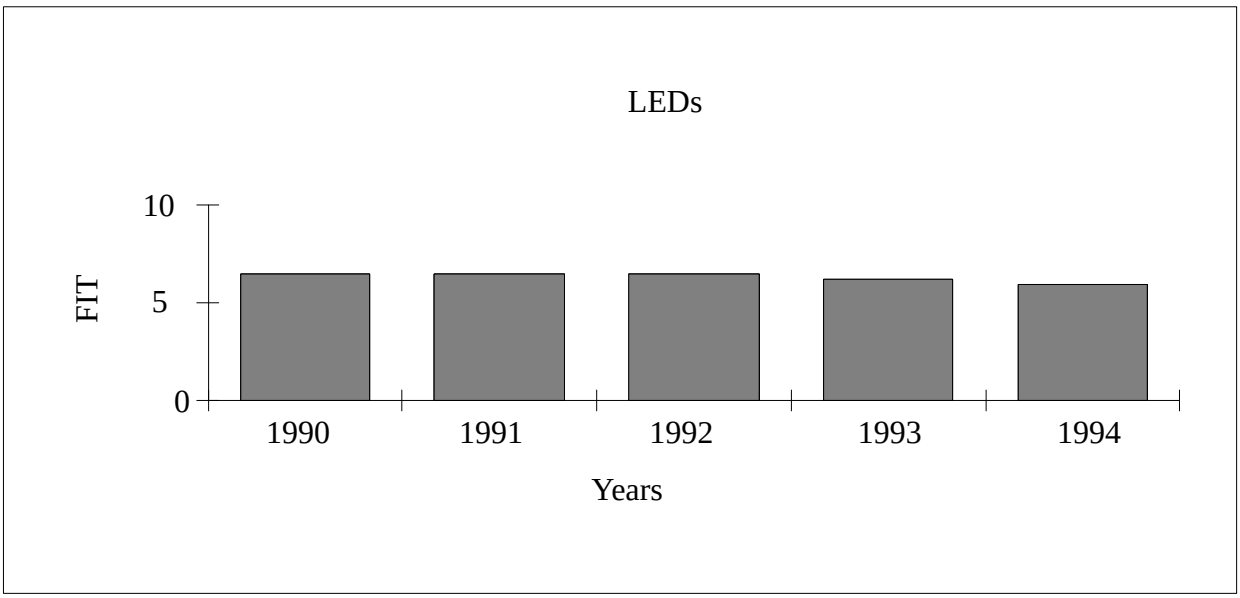


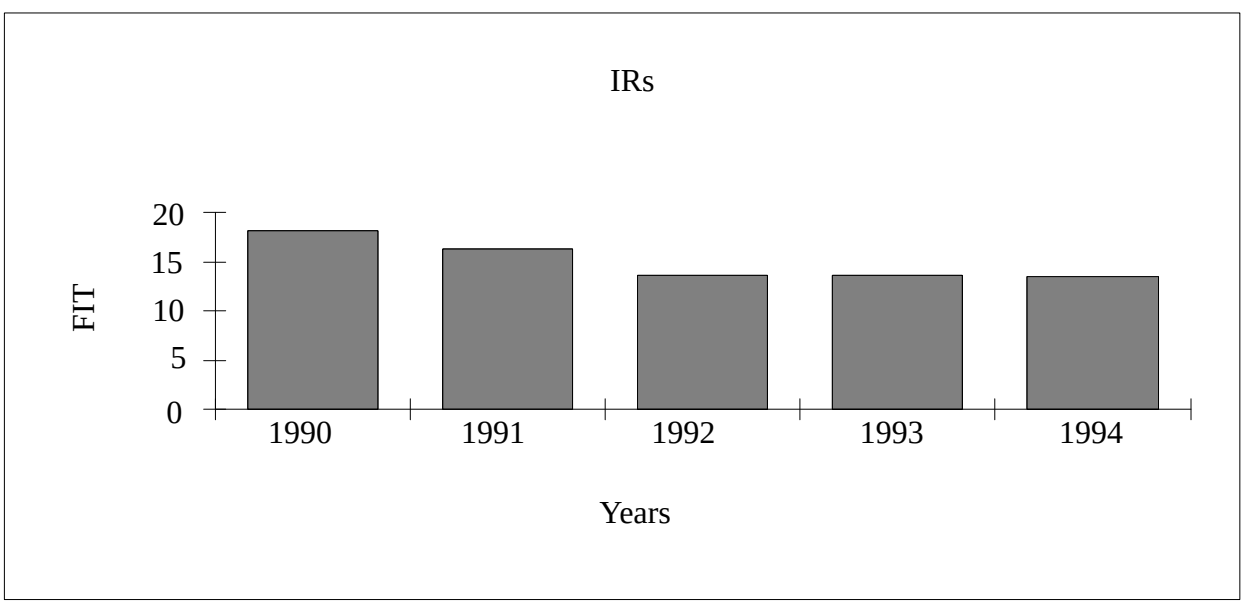


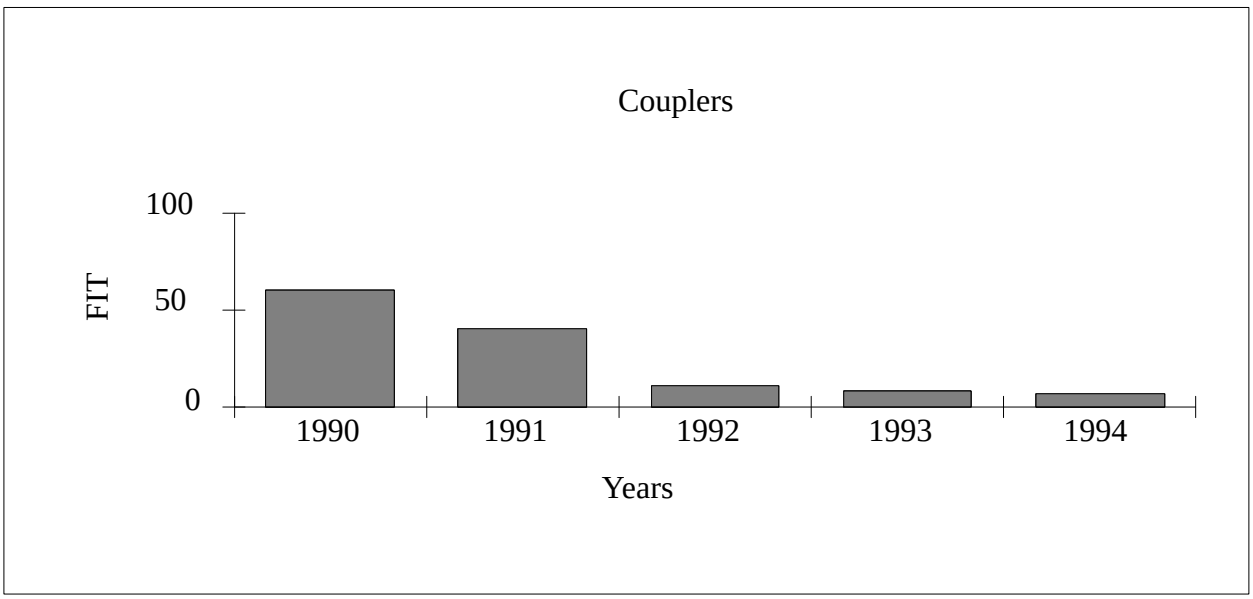
EFR-Values Opto Components

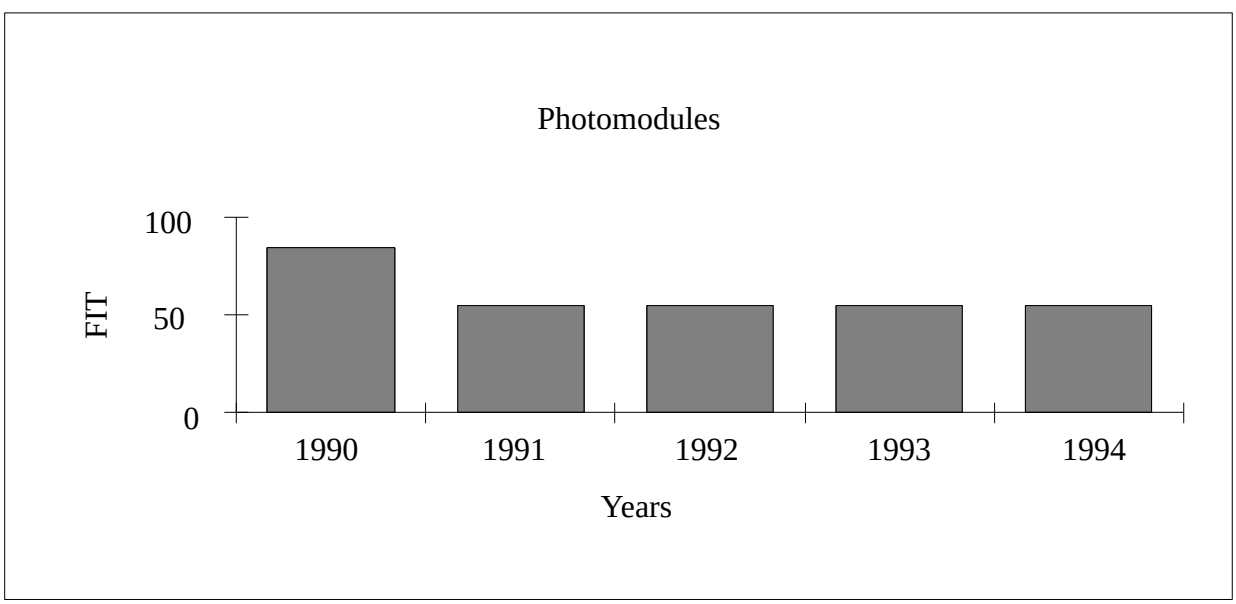
Test	Technology	Sample Size	Failures	Failure Rate in ppm
Operating life	Couplers	2300	0	0
	IRs	2250	2	889
	LEDs	4850	2	412
	Photomodules	850	0	0
	Opto total	10250	4	390

FIT-Values Opto Components






Couplers
100
50
0
FIT
1990
1991
1992
1993
1994
Years


Photomodules
100
50
0
FIT
1990
1991
1992
1993
1994
Years